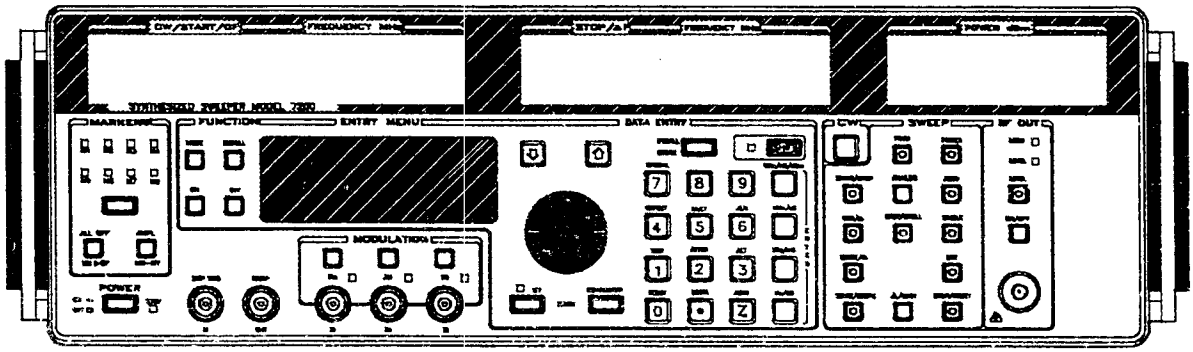
Giga-tronics

OPERATION & MAINTENANCE MANUAL

MODEL 7200

Synthesized Microwave Sweeper



Volume 2 of 2

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WARRANTY

Giga-tronics Model 7200 instruments are warranted against defective materials and workmanship for three years from date of shipment. Giga-tronics will at its option repair or replace products that are proven defective during the warranty period.

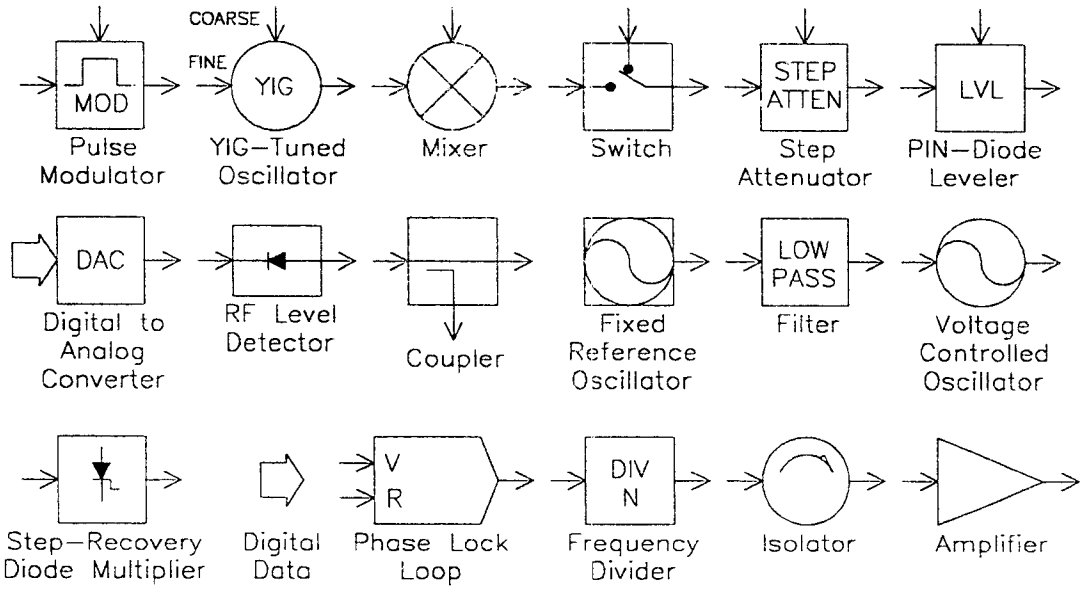
This warranty DOES NOT cover damage resulting from improper use, nor workmanship other than Giga-tronics service.

There is no implied warranty of fitness for a particular purpose, nor is Giga-tronics liable for any consequential damages.

Specification and price change privileges are reserved by Giga-tronics.

SYMBOLS

Block diagram symbols frequently used in the manual are illustrated below.



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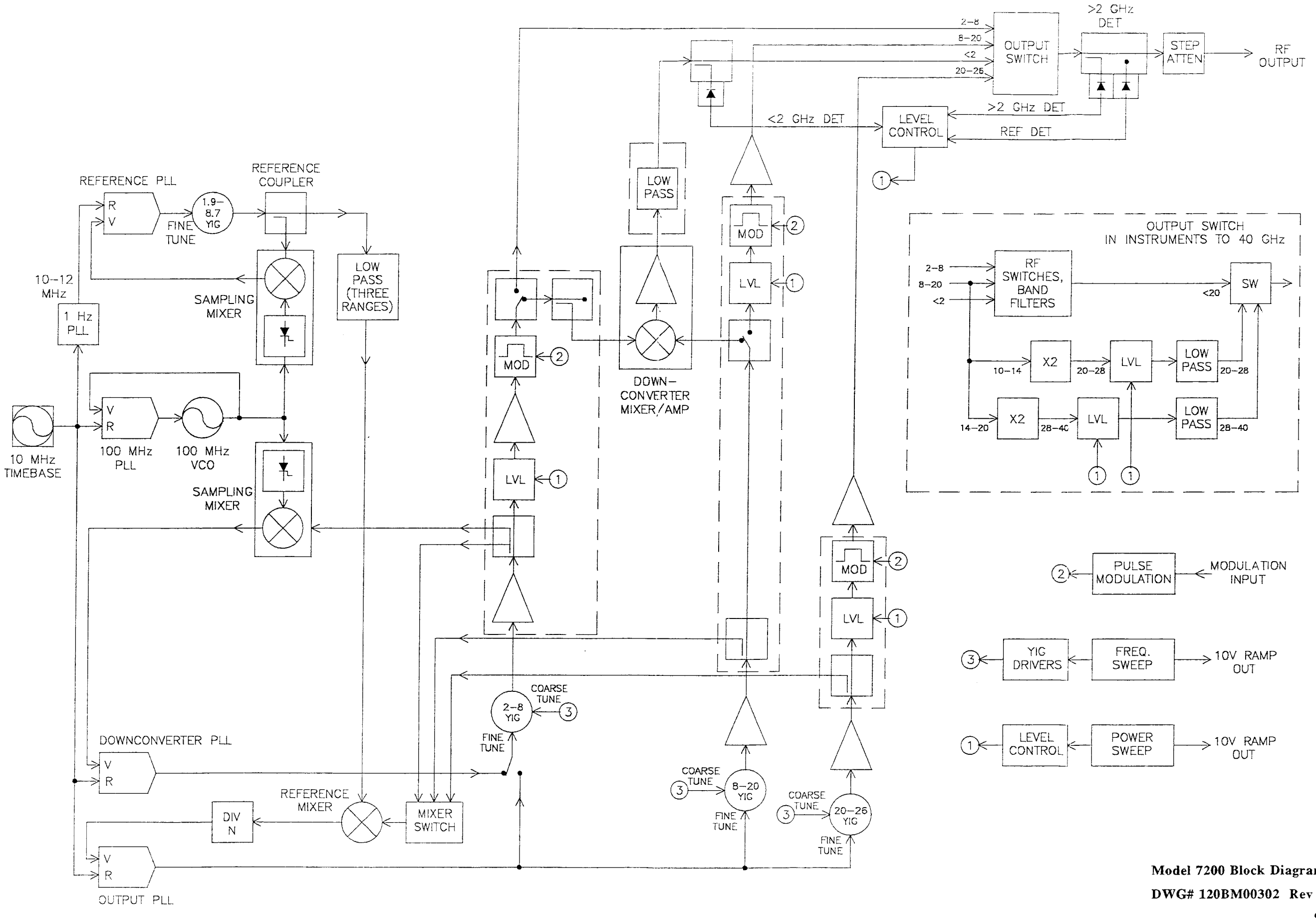
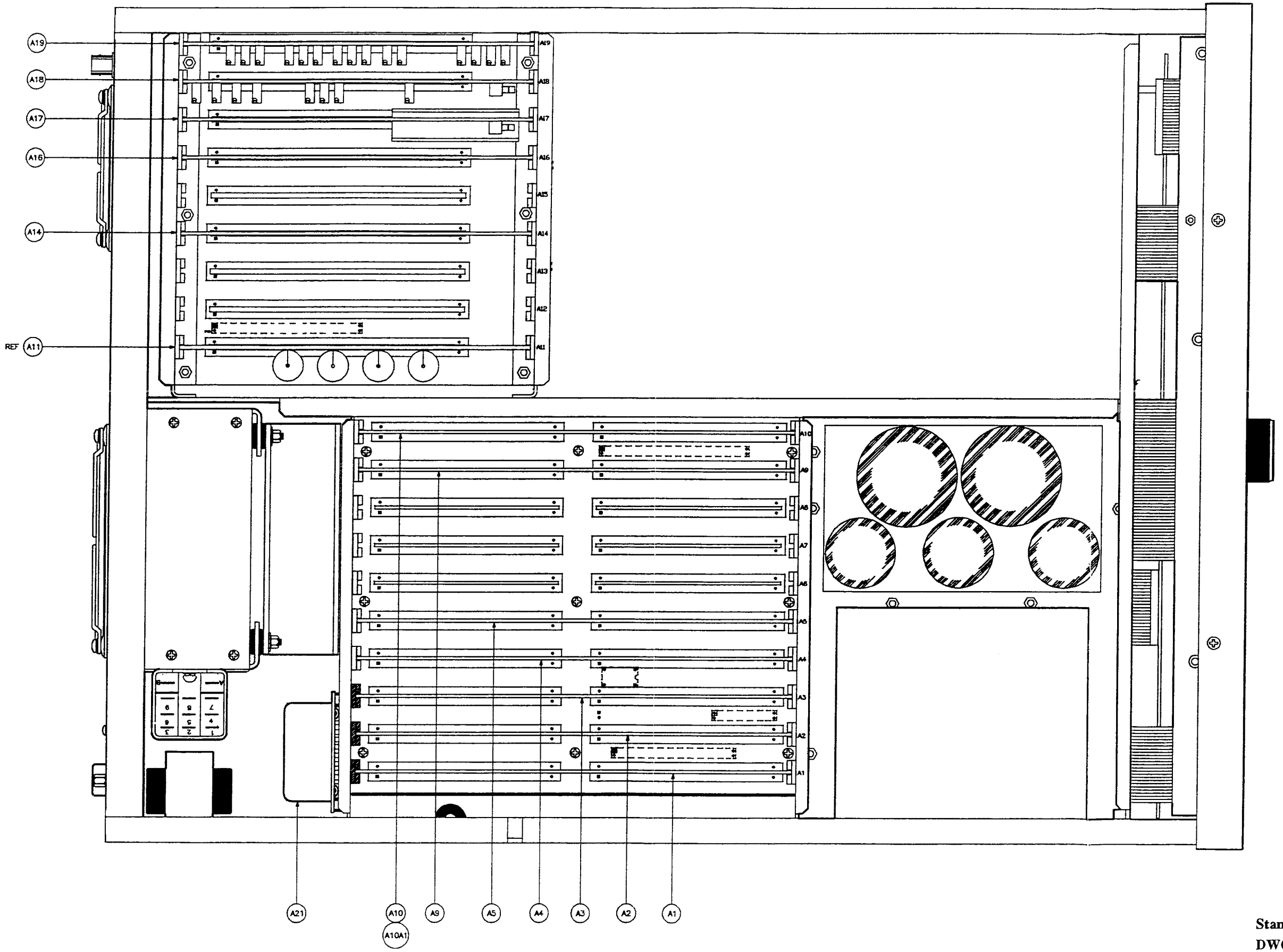
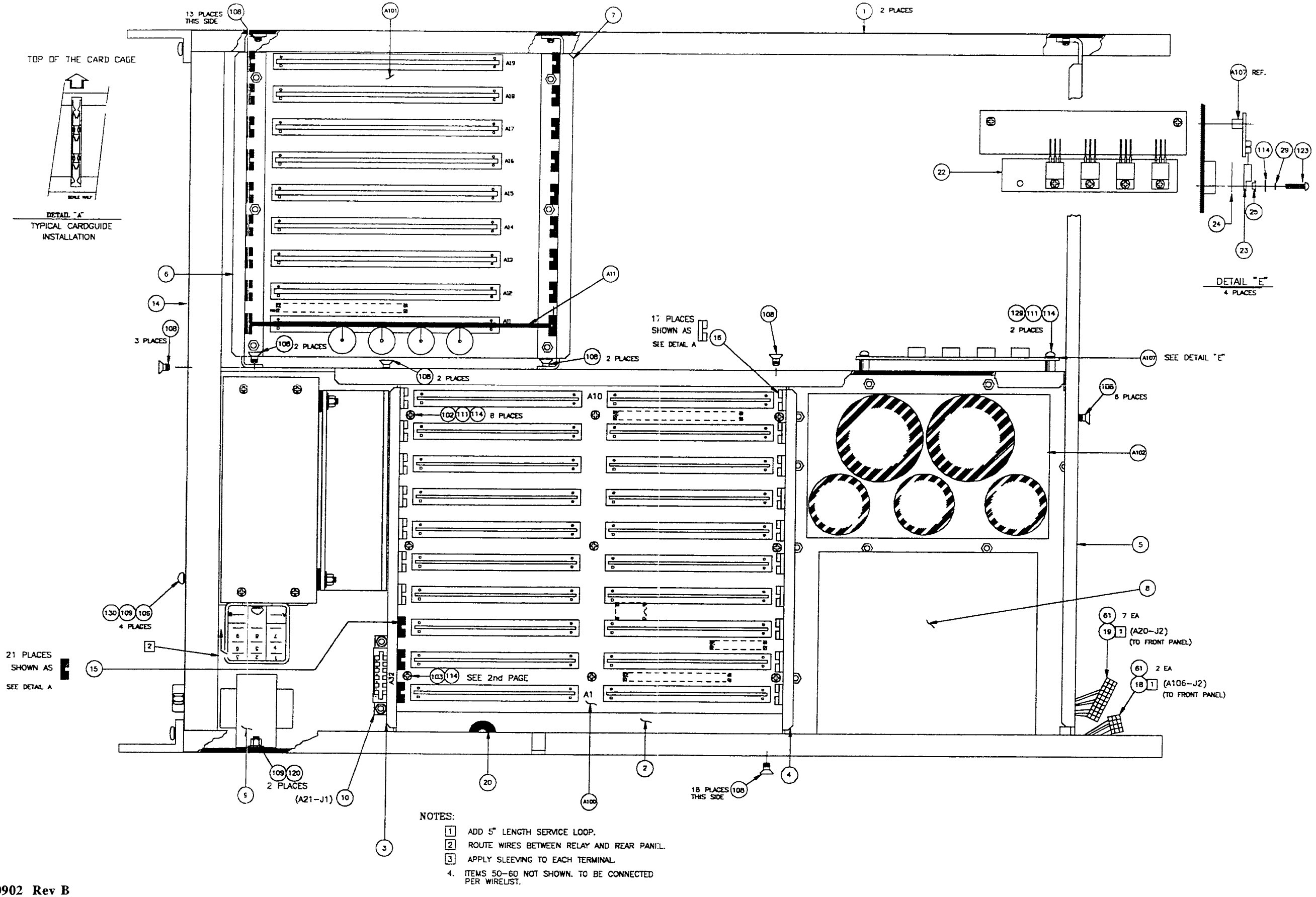


Model 7200 Block Diagram

DWG# 120BM00302 Rev B

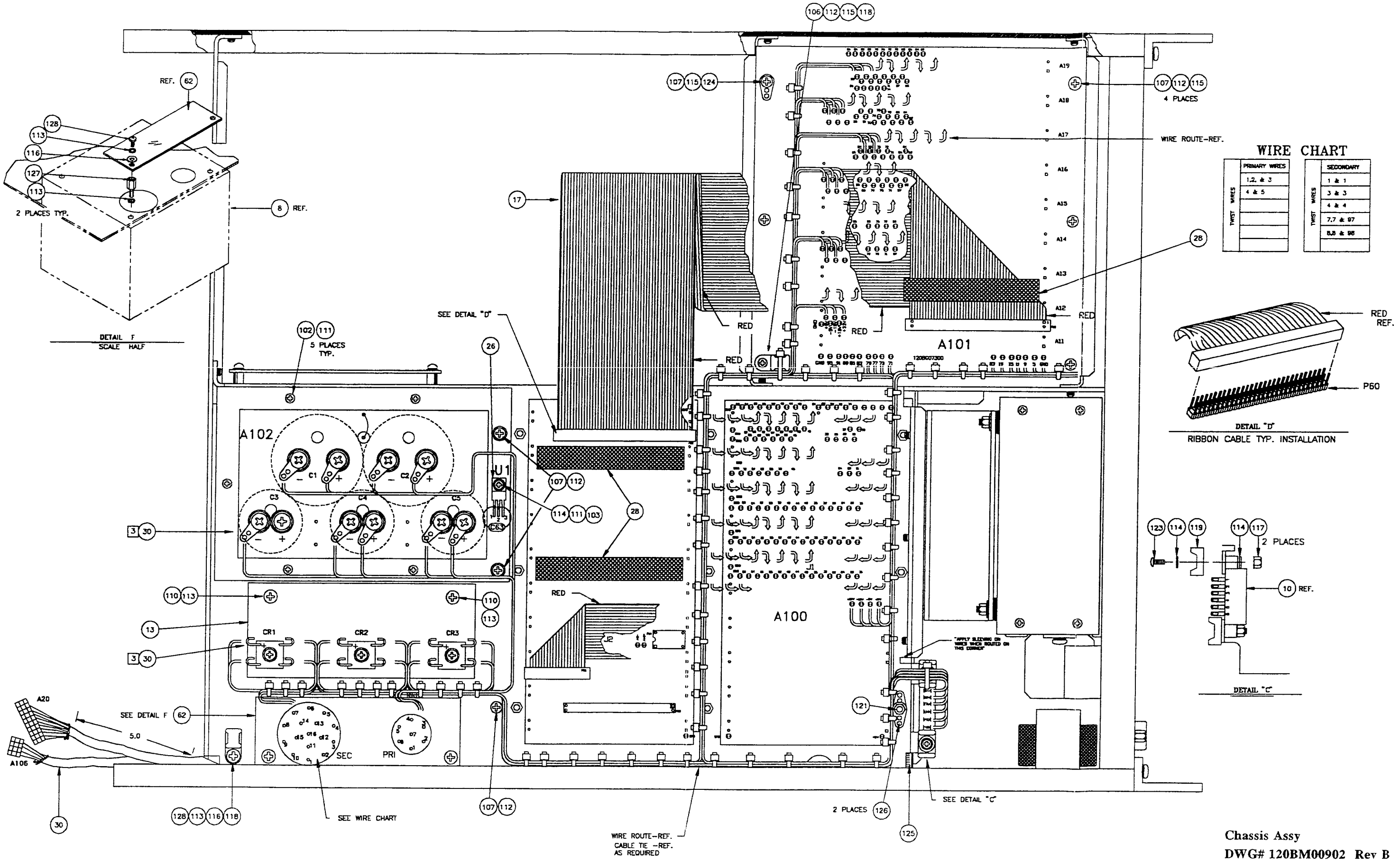


Standard PCB Assy
DWG# 120BM00700 Rev H
Sheet 1 of 1

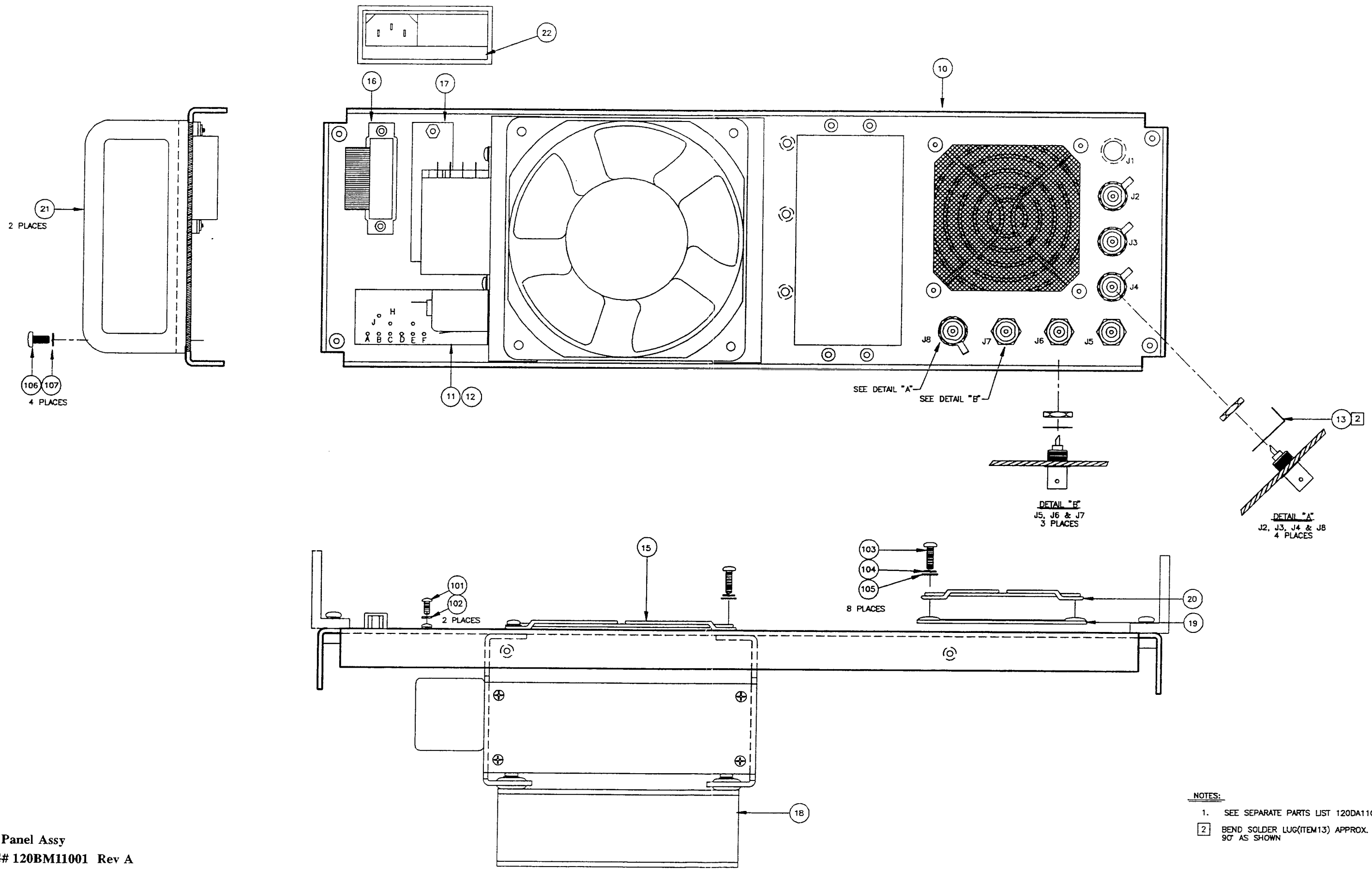


NOTES:

1. ADD 5" LENGTH SERVICE LOOP.
2. ROUTE WIRES BETWEEN RELAY AND REAR PANEL.
3. APPLY SLEEVING TO EACH TERMINAL.
4. ITEMS 50–60 NOT SHOWN. TO BE CONNECTED PER WIRELIST.



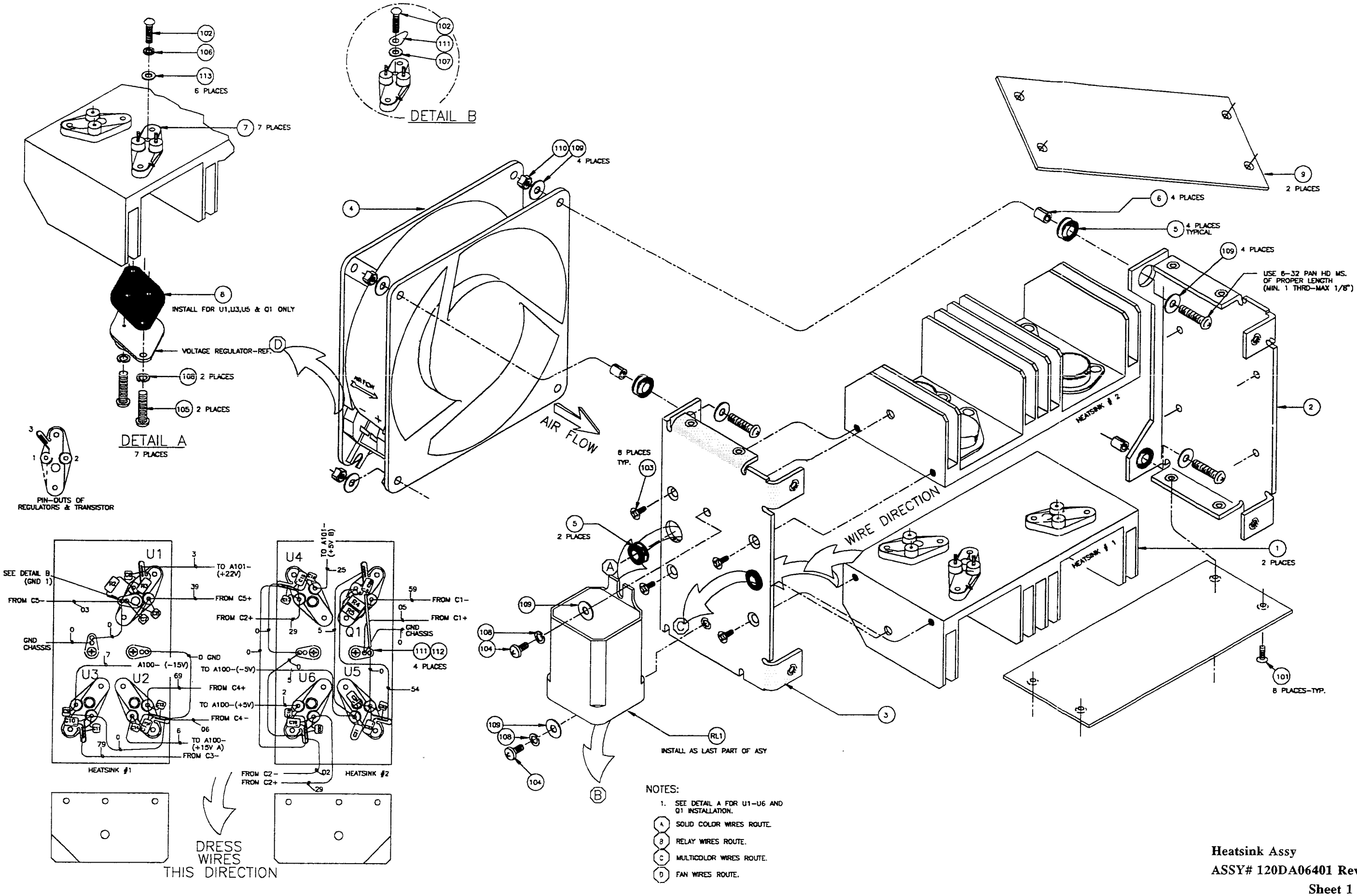
Chassis Assy
DWG# 120BM00902 Rev B
Sheet 2 of 2
7-4



NOTES:

1. SEE SEPARATE PARTS LIST 120DA11001
2. BEND SOLDER LUG(ITEM13) APPROX. 90° AS SHOWN

Rear Panel Assy
DWG# 120BM11001 Rev A
Sheet 1 of 1
7-5



NOTES:

1. SEE DETAIL A FOR U1–U6 AND Q1 INSTALLATION.

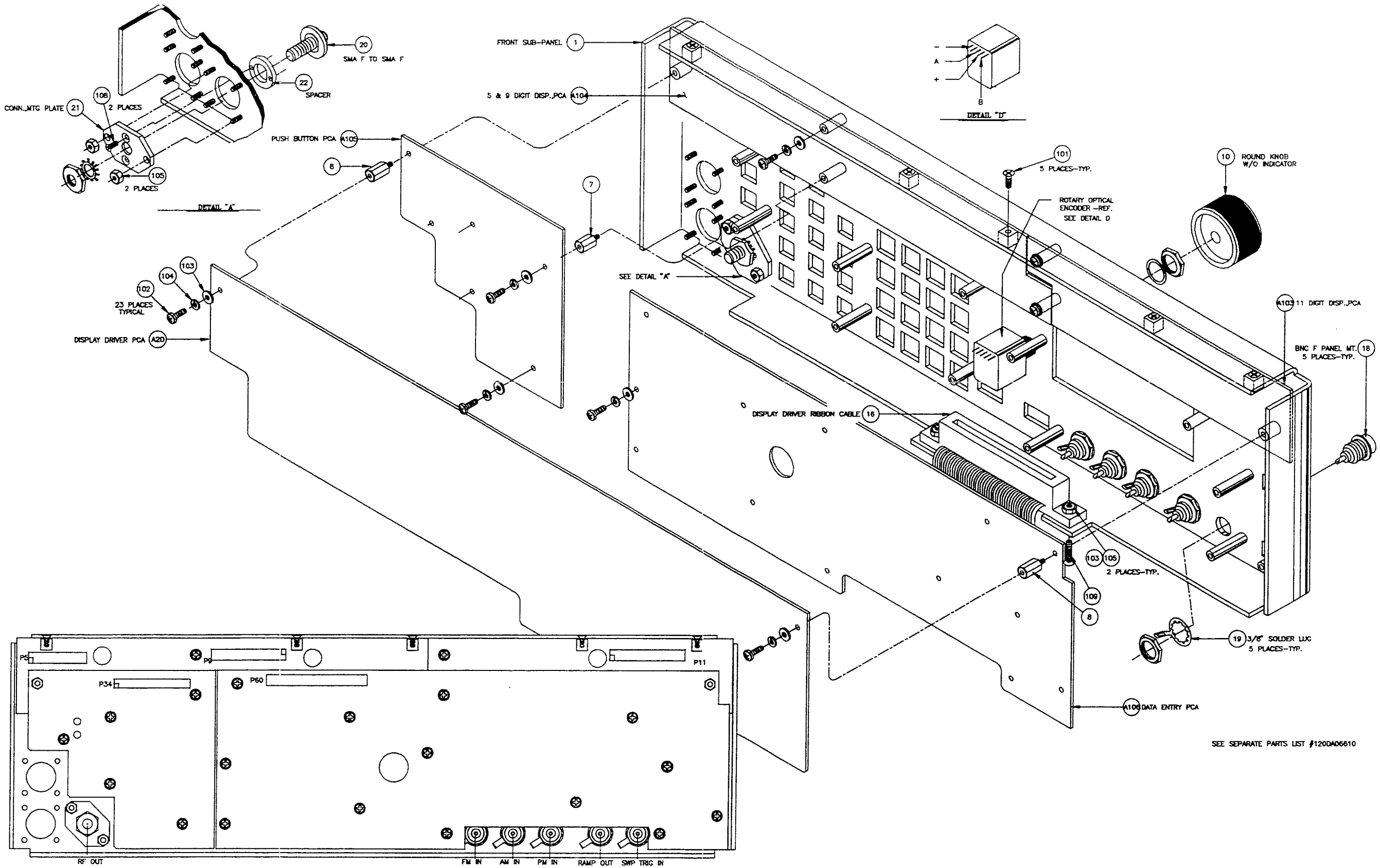
A SOLID COLOR WIRES ROUTE.

B RELAY WIRES ROUTE.

C MULTICOLOR WIRES ROUTE.

D FAN WIRES ROUTE.

Heatsink Assy
ASSY# 120DA06401 Rev A
Sheet 1 of 1



Front Panel Assy
DWG# 120BM06610 Rev A
Sheet 1 of 2
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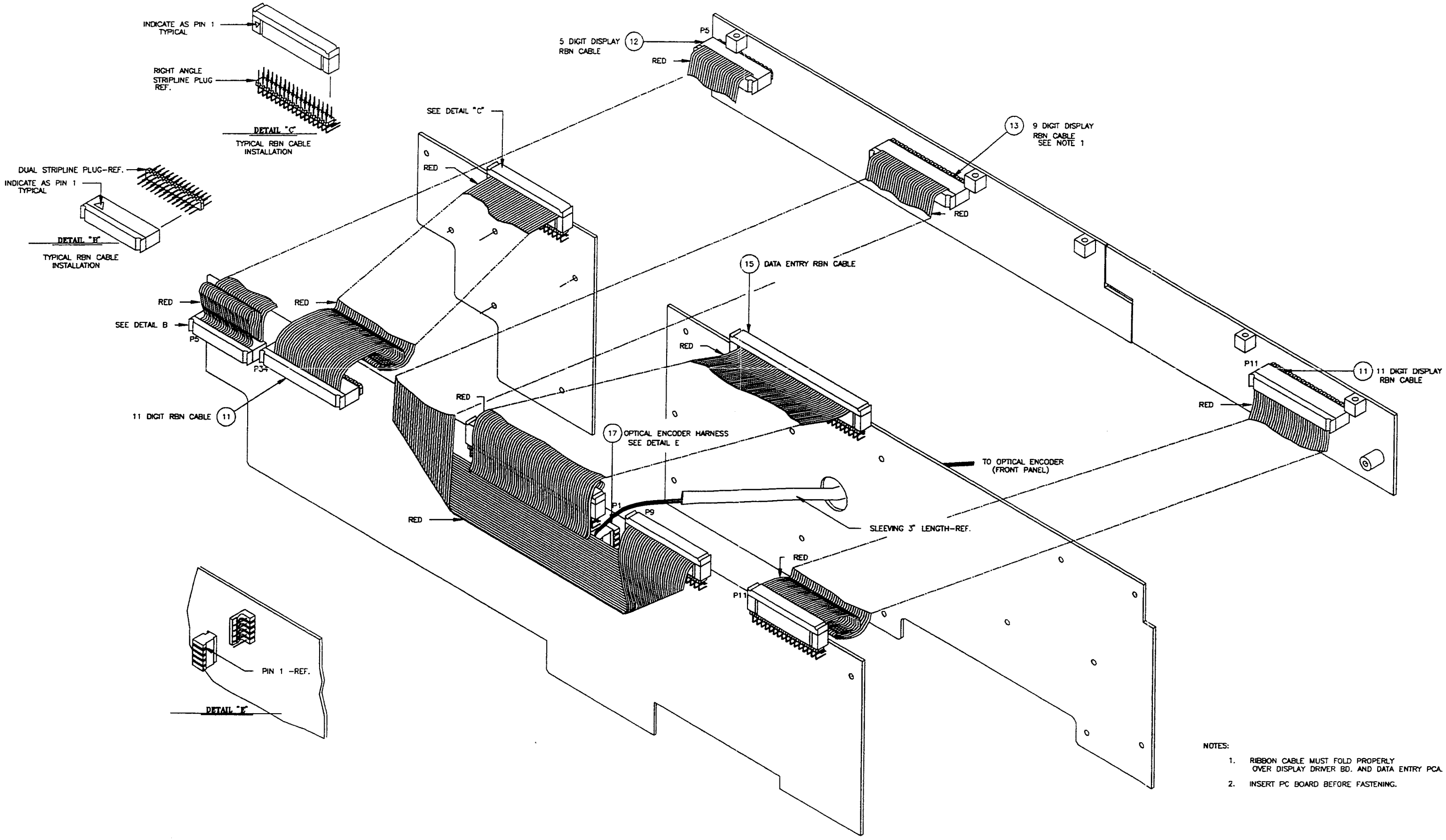
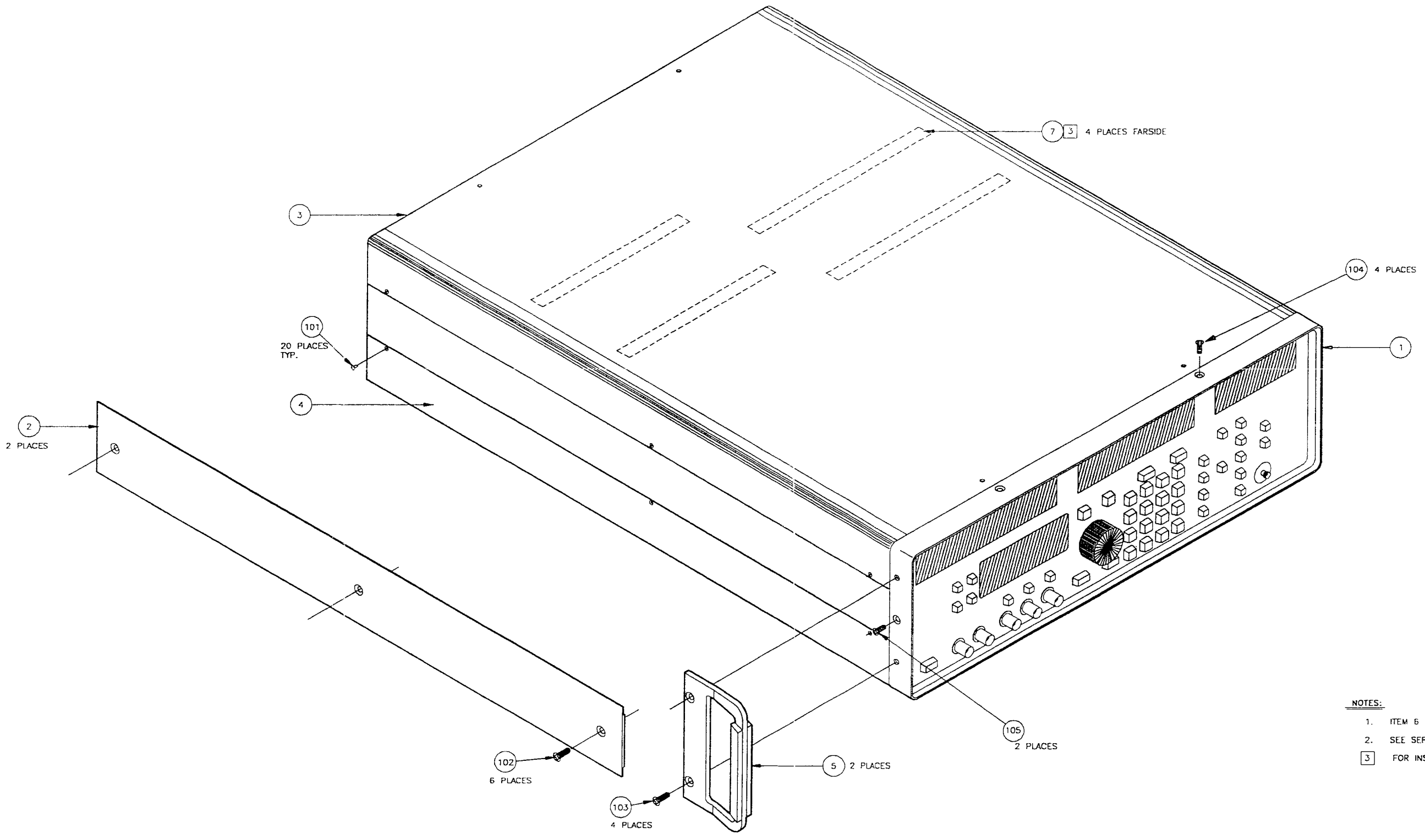


NOTES:

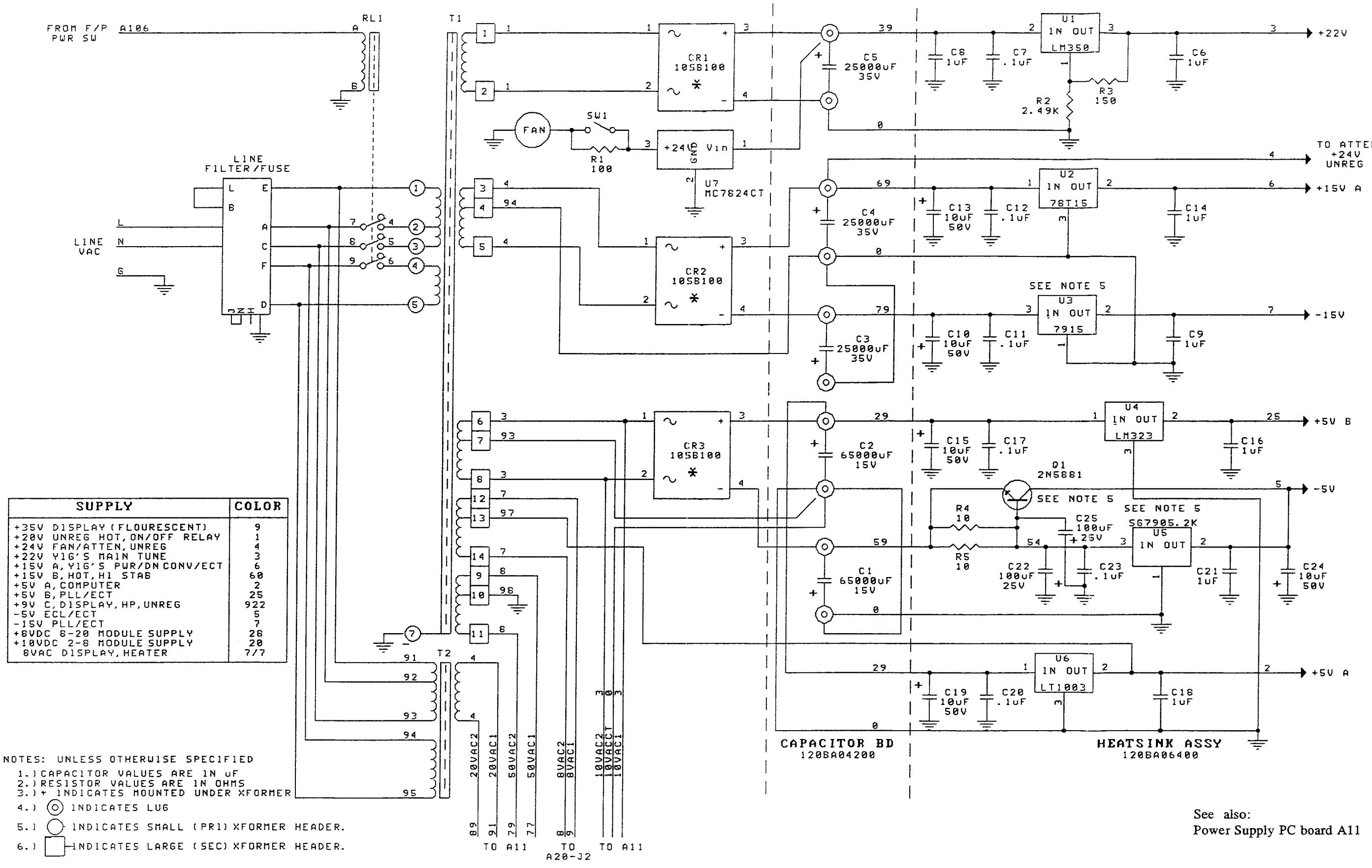
1. RIBBON CABLE MUST FOLD PROPERLY OVER DISPLAY DRIVER BD. AND DATA ENTRY PCA.
2. INSERT PC BOARD BEFORE FASTENING.



NOTES:

1. ITEM 6 NOT SHOWN
2. SEE SEPARATE P/L 120DA11200
3. FOR INSTALLATION SEE 002CF03600

Bench Mount Dress Assy
ASSY# 120DA11200 Rev D
Sheet 1 of 1



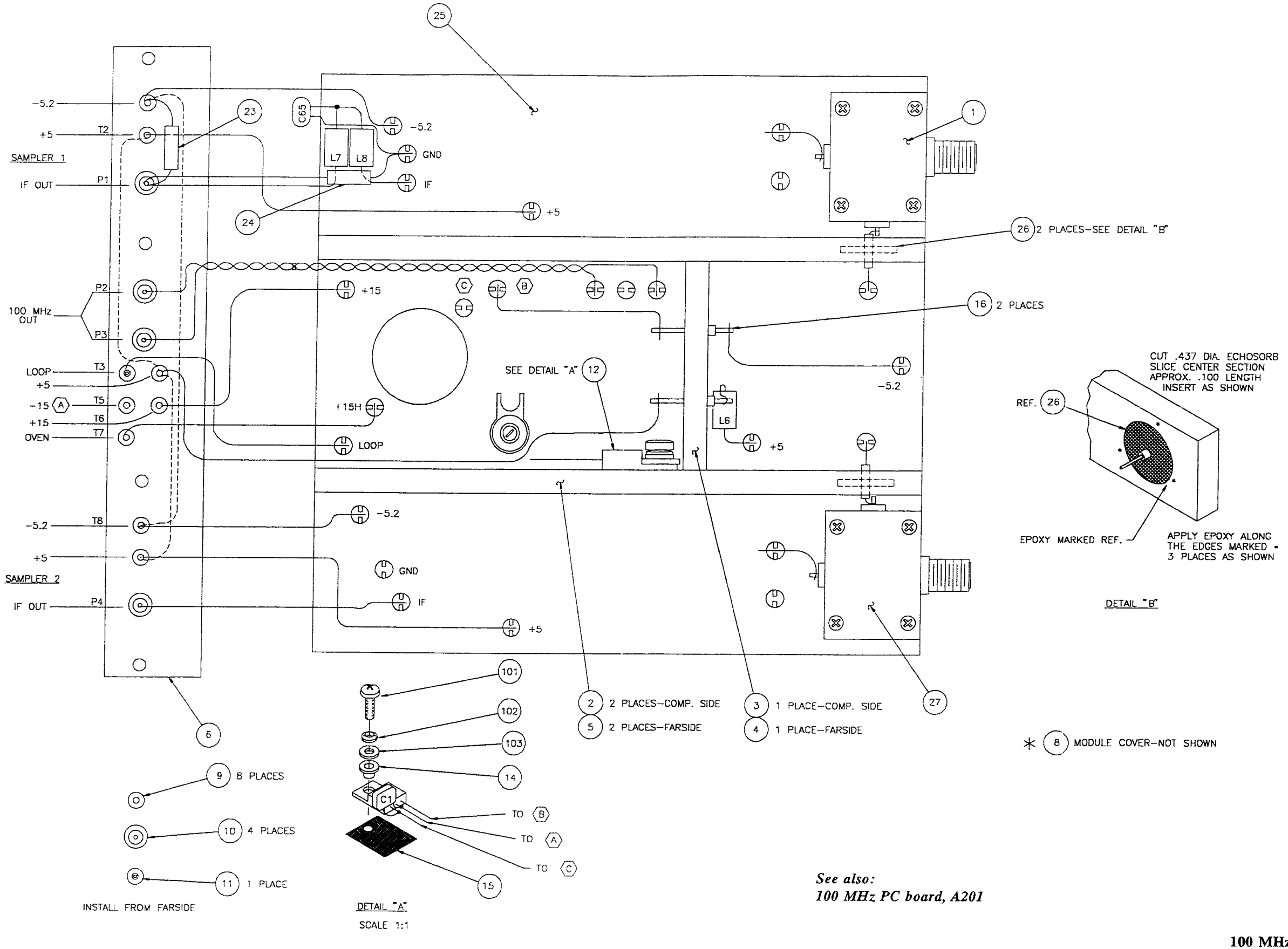
SUPPLY	COLOR
+35V DISPLAY (FLOURESCENT)	9
+20V UNREG HOT, ON/OFF RELAY	1
+24V FAN/ATTEN, UNREG	4
+22V YIG'S MAIN TUNE	3
+15V A, YIG'S PWR/DN CONV/ECT	6
+15V B, HOT, H1 STAB	60
+5V A, COMPUTER	2
+5V B, PLL/ECT	25
+9V C, DISPLAY, HP, UNREG	922
-5V ECL/ECT	5
-15V PLL/ECT	7
+8VDC 8-20 MODULE SUPPLY	26
+10VDC 2-8 MODULE SUPPLY	20
8VAC DISPLAY, HEATER	7/7

NOTES: UNLESS OTHERWISE SPECIFIED

1.) CAPACITOR VALUES ARE IN uF
2.) RESISTOR VALUES ARE IN OHMS
3.) + INDICATES MOUNTED UNDER XFORMER
4.) ⊙ INDICATES LUG
5.) ○ INDICATES SMALL (PRI) XFORMER HEADER.
6.) ⊣ INDICATES LARGE (SEC) XFORMER HEADER.

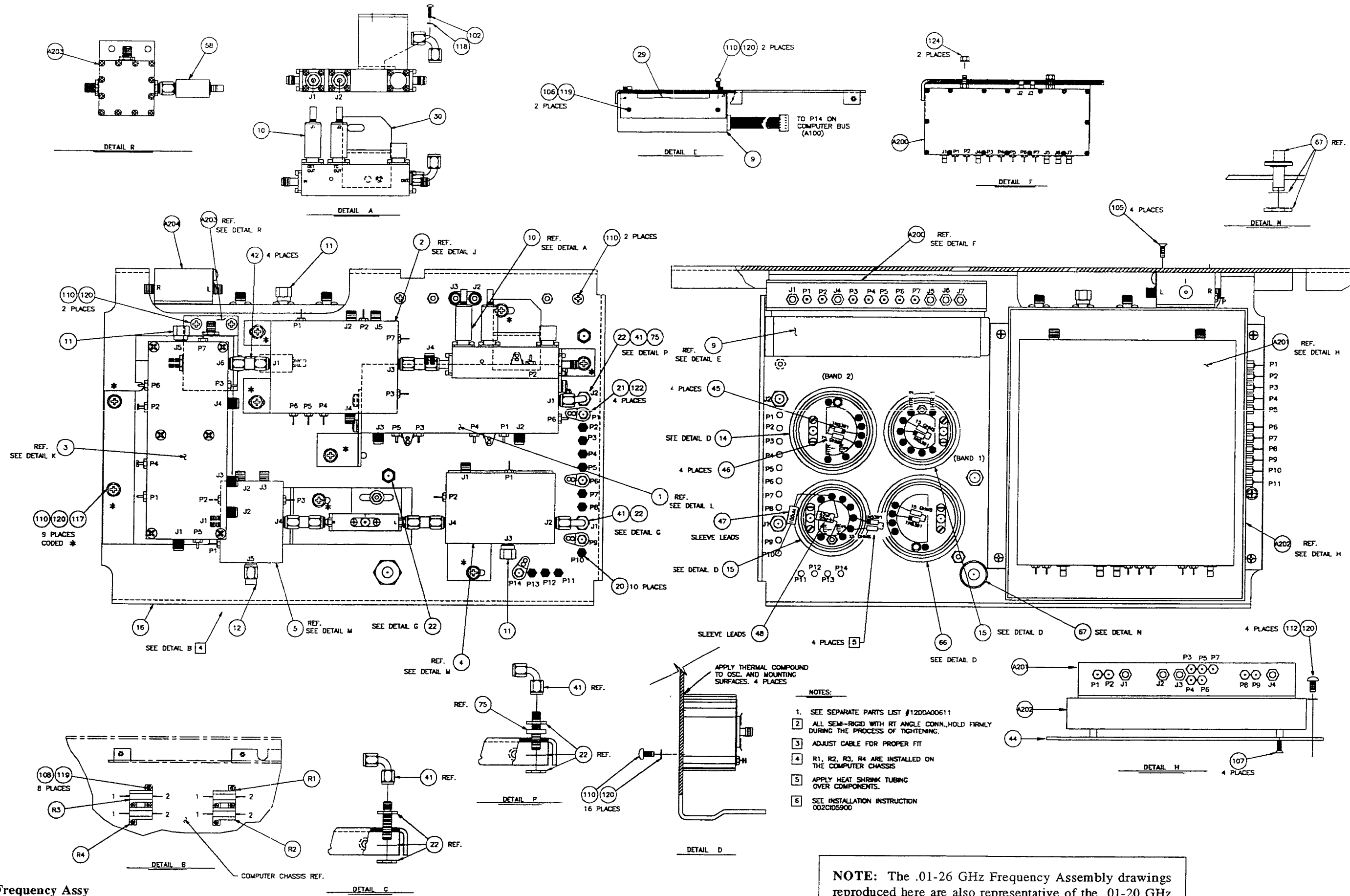
See also:
Power Supply PC board A11

Power Supply #2
DWG# 120BM05400 Rev H
Sheet 1 of 1
7-10



See also:
100 MHz PC board, A201

100 MHz Module Assy (A201)
ASSY# 120CA11500 Rev F
Sheet 1 of 1
7-11

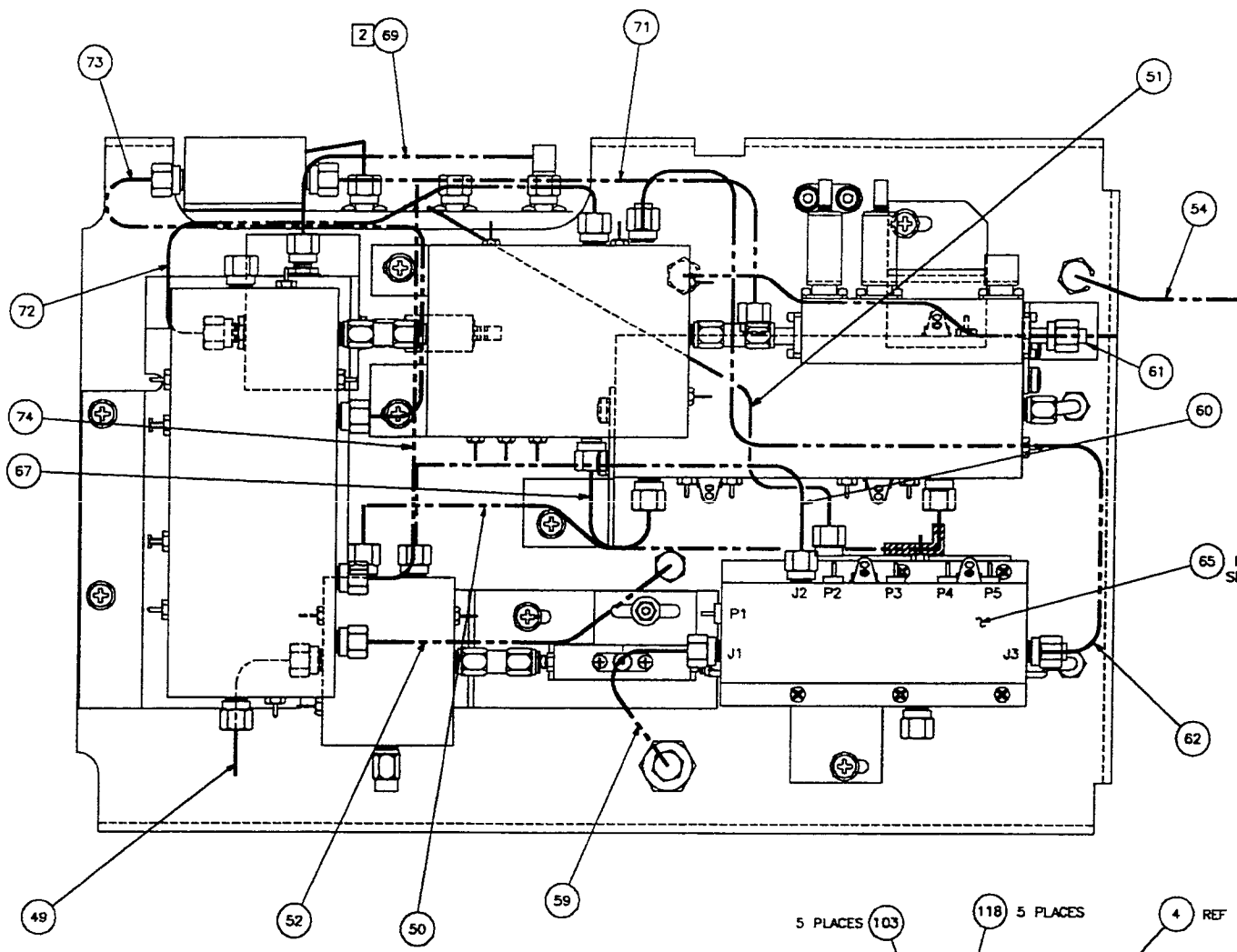


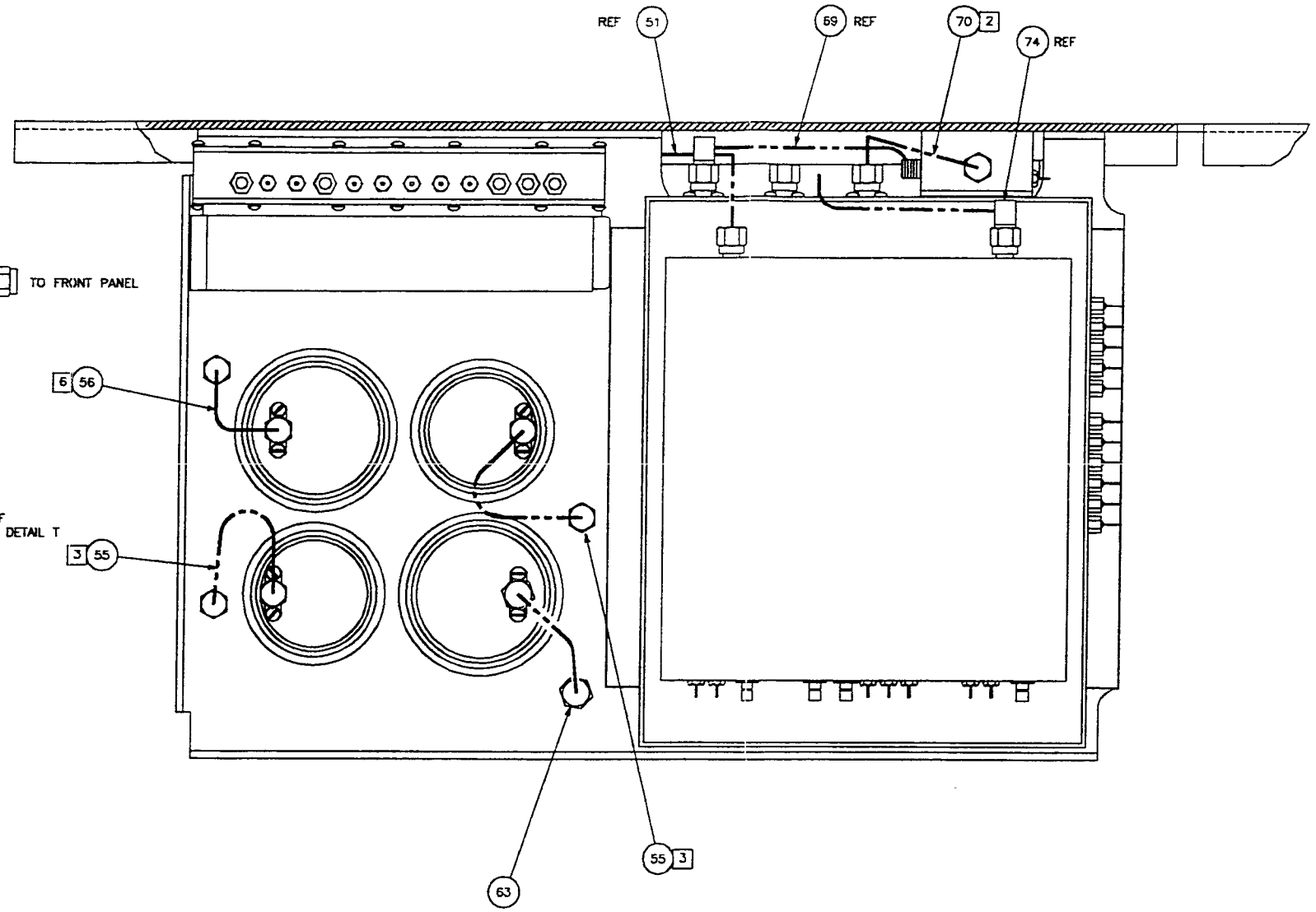
NOTES:

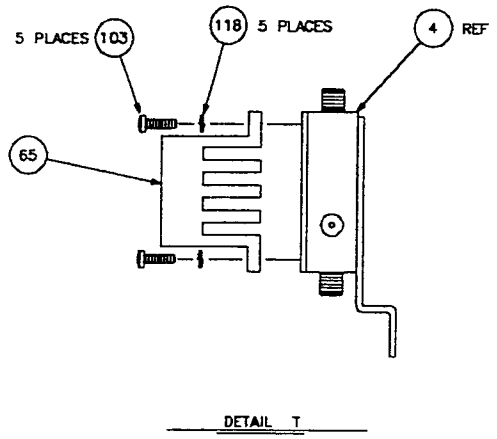
1. SEE SEPARATE PARTS LIST #120DA00611
2. ALL SEMI-RIGID WITH RT ANGLE CONN., HOLD FIRMLY DURING THE PROCESS OF TIGHTENING.
3. ADJUST CABLE FOR PROPER FIT
4. R1, R2, R3, R4 ARE INSTALLED ON THE COMPUTER CHASSIS
5. APPLY HEAT SHRINK TUBING OVER COMPONENTS.
6. SEE INSTALLATION INSTRUCTION 002CI05900

.01-26 GHz Frequency Assy
ASSY# 120DA00611 Rev D
Sheet 1 of 3
7-12

NOTE: The .01-26 GHz Frequency Assembly drawings reproduced here are also representative of the .01-20 GHz frequency assembly. See the parts lists of these assemblies in Section 6 of the manual for component differences.







DETAIL T

.01-26 GHz Frequency Assy
ASSY# 120DA00611 Rev D
Sheet 2 of 3
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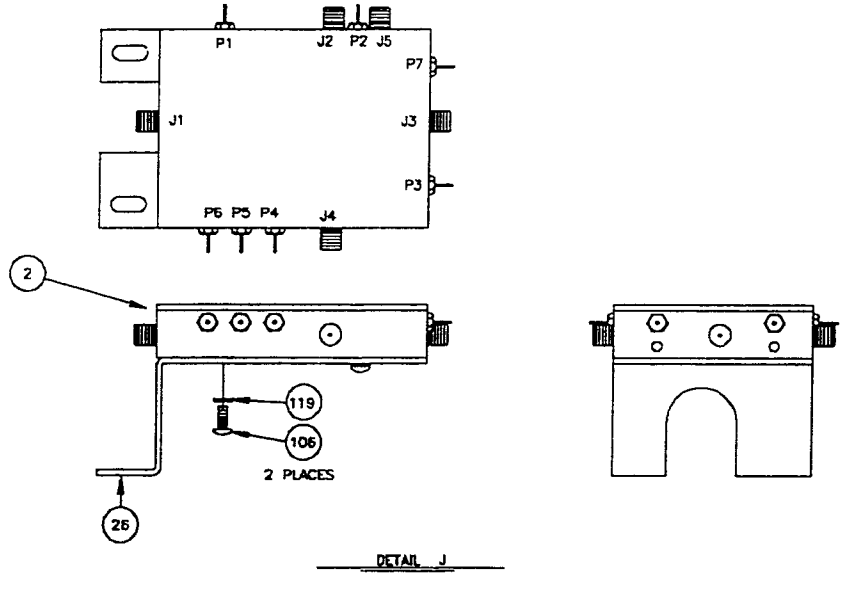
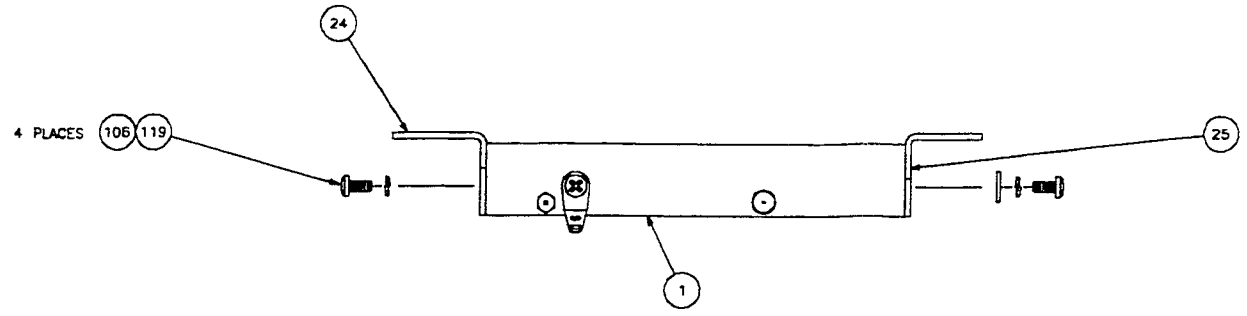
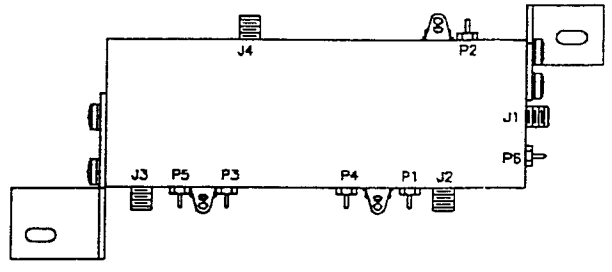
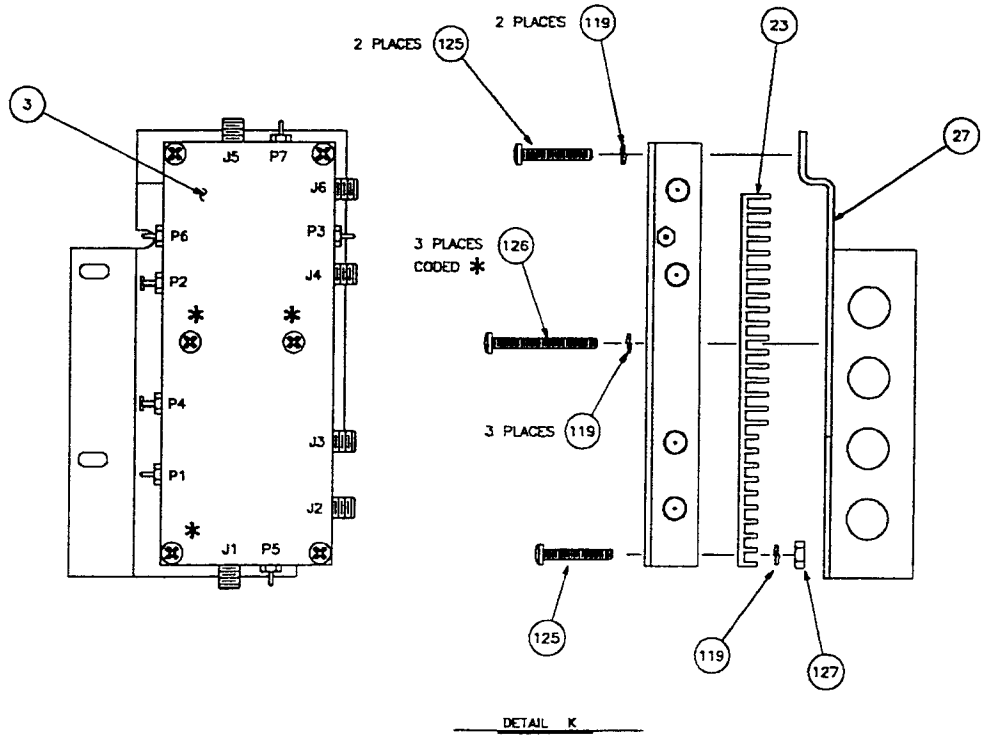


DETAIL J

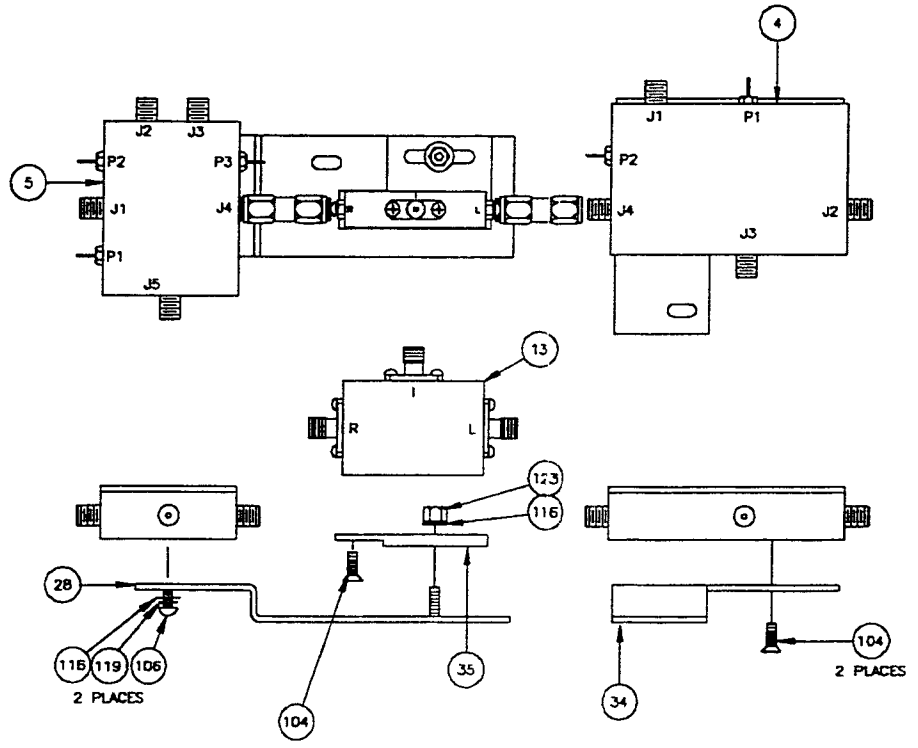




DETAIL L



DETAIL K



DETAIL M

.01-26 GHz Frequency Assy
ASSY# 120DA00611 Rev D
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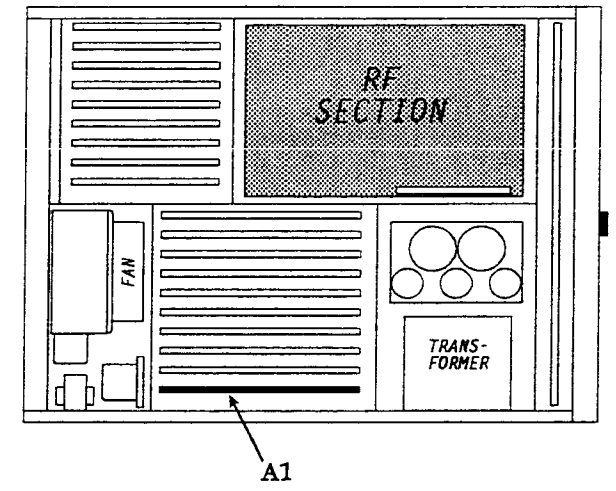
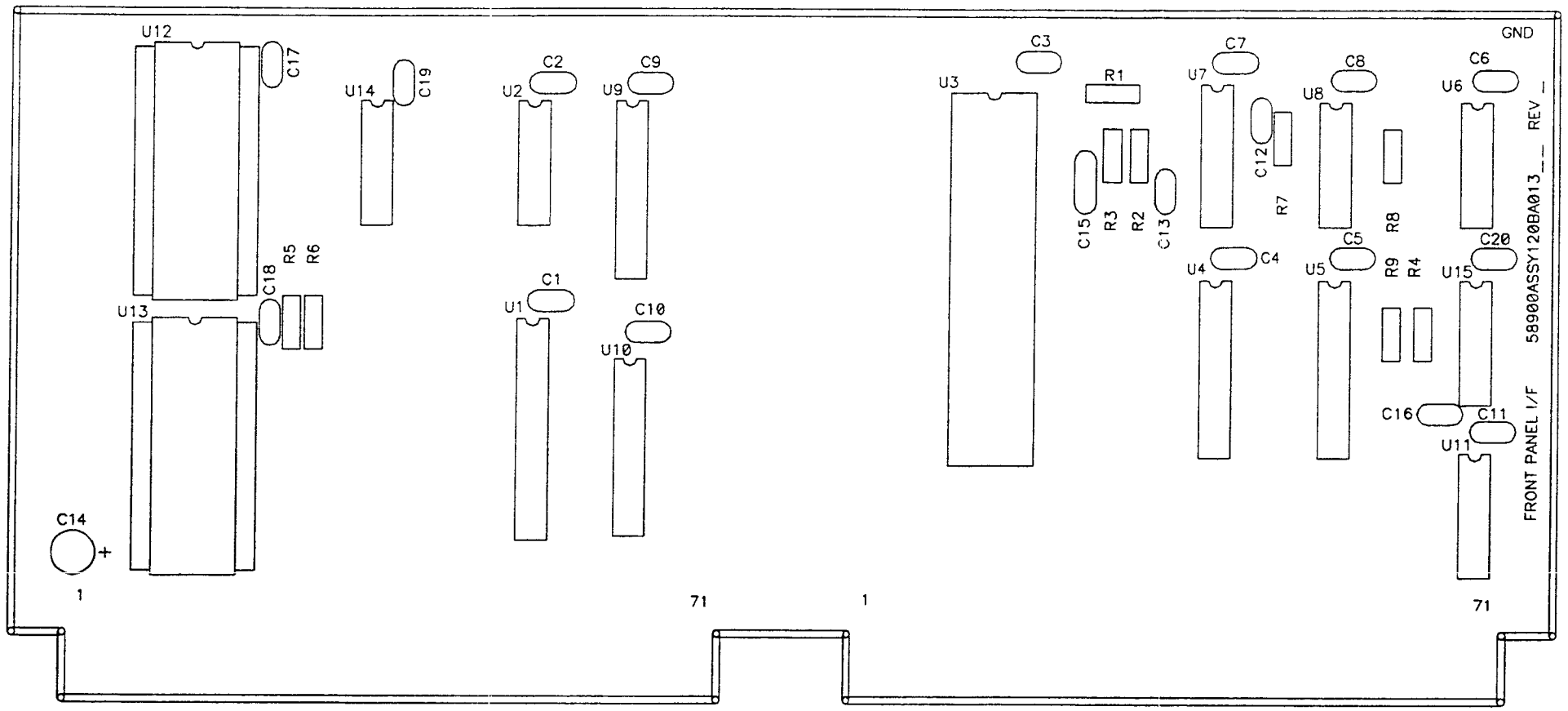


Front Panel Interface (A1)
DWG# 120BM01300 Rev C
Sheet 1 of 4
7-A1-1



FRONT PANEL INTERFACE -- PC ASSY A1

As the name implies, the Front Panel Interface PCA provides for all interface between the front panel and computer. This includes front panel data entry (in the form of keystrokes or knob movement) as well as front panel data display.

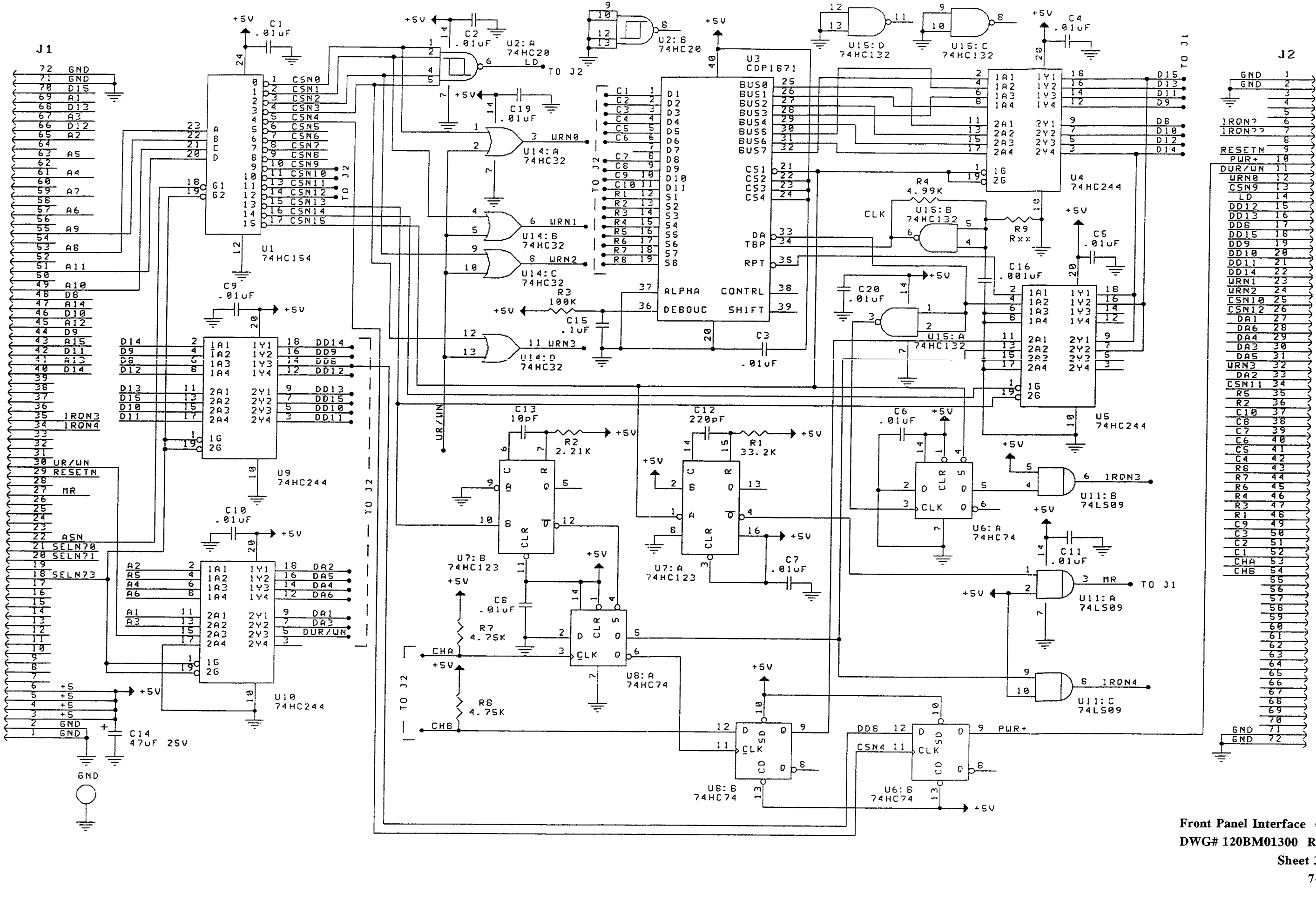
U1, a 4 to 16 decoder, decodes the chip selects for the different front panel displays and interfaces. U14 A thru D provide the individual chip selects for the front panel 'Entry Menu' displays, which are gated by the UR/UN line. U2 A provides a load signal for loading data to these displays.

The U3 Keyboard decoder, where D1-11 represent columns and S1-8 are rows, identifies keys pressed and outputs information to the computer bus via U5 buffer. U15 B provides a clock circuit for scanning the keyboard. Whenever keyboard is active, U15 A detects the data available line and causes an interrupt to be generated by U6 A, U11 B. When the computer responds with a chip select from U1 indicating that the keyboard can be read, the interrupt is cleared via U6 A. U7 A and U11 A activate the memory ready line which slows the CPU as required for read cycles to take place.

Any time the front panel knob is turned, the optical decoder generates pulses which are seen at U8 A and B; the flip flops of U8 are set up such that the output at U8-9 indicates which way the knob was turned. U8-5 flips, generating an interrupt via U11 C. When the computer selects the knob to be read a chip select is received at U7-B, from U1, which clears the interrupt.

U4, U5, U9, and U18 provide buffers for computer bus interface.

On the next page of the diagram, U12 is the 'CONFIGURATION' ROM, which stores the information about the unit such as its frequency range and what options it has. It is also programmed to hold various characterization data. U13 is a non-volatile RAM chip which is used to store the current unit settings when the power is turned off. It is also used to store multiple unit setups in memory locations 0 thru 9.



Front Panel Interface (A1)
DWG# 120BM01300 Rev C
Sheet 3 of 4
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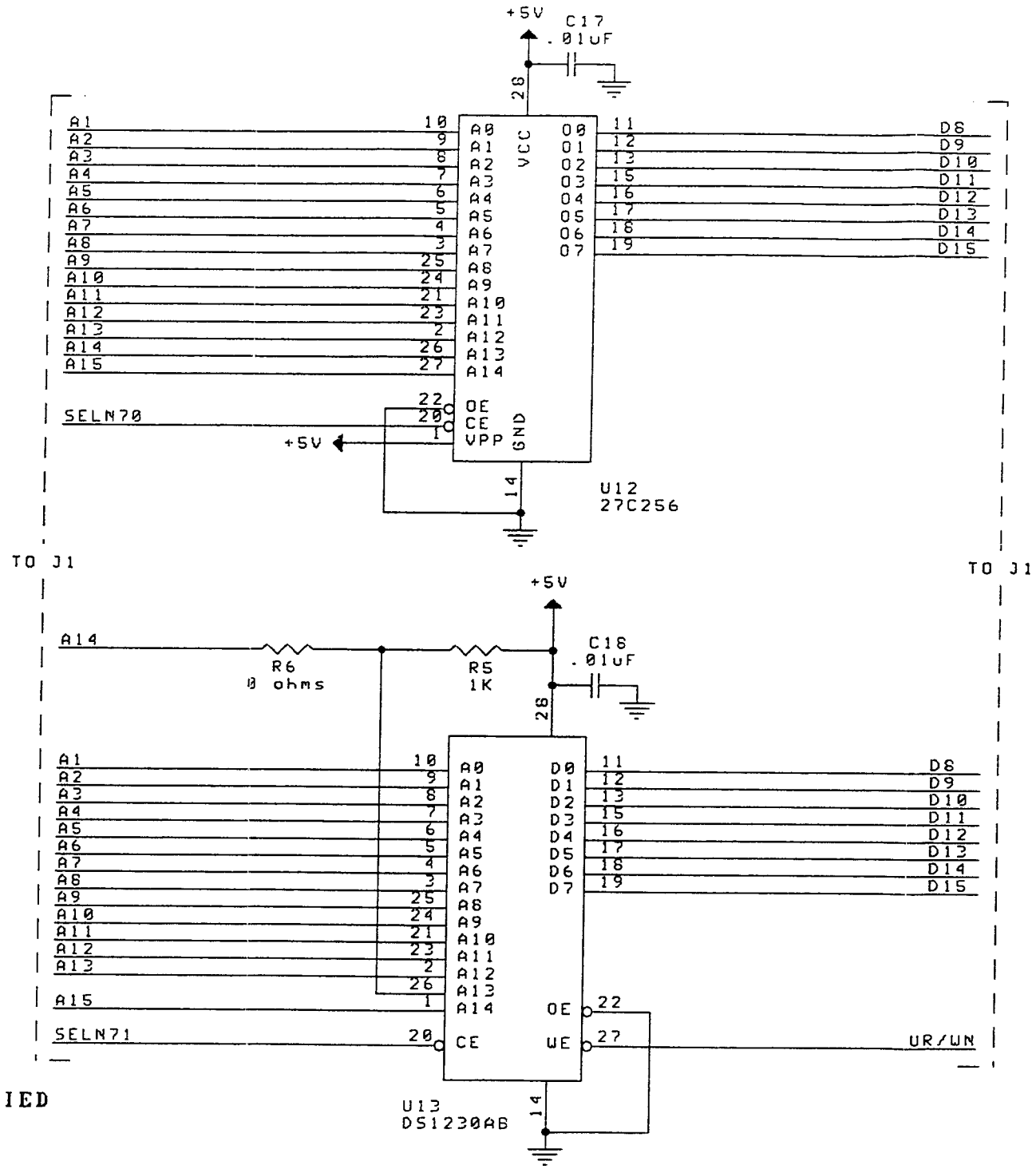
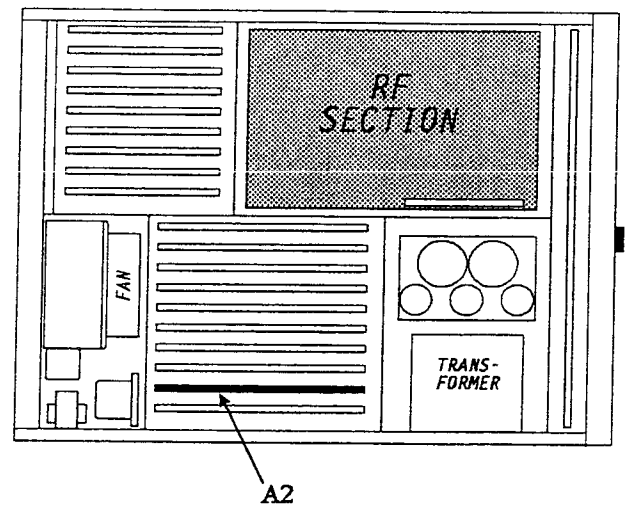
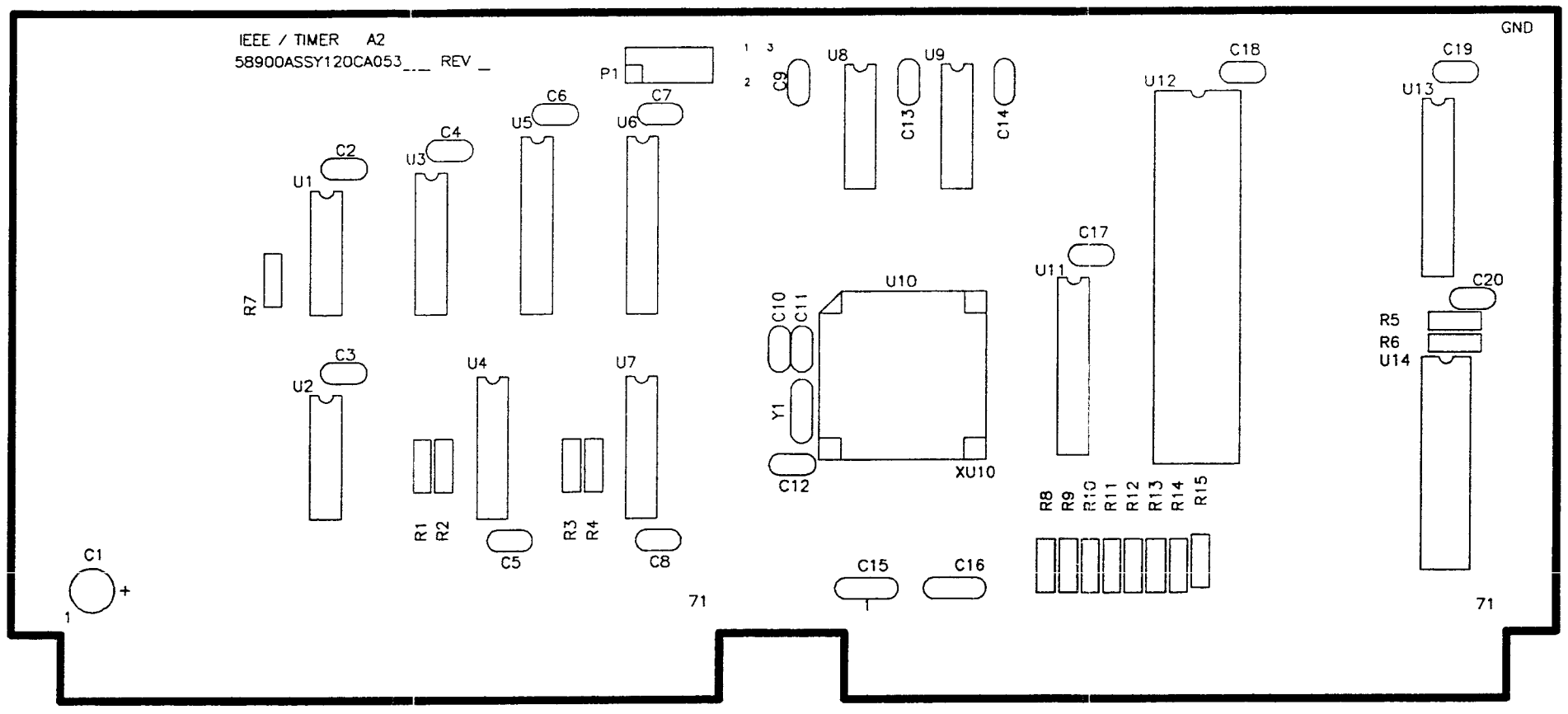


NOTES: UNLESS OTHERWISE SPECIFIED

1.) CAPACITOR VALUES ARE IN uF
2.) RESISTOR VALUES ARE IN OHMS
3.) RESISTORS ARE 1/4W, 1%



IEEE/Timer (A2)
DWG# 120BM05300 Rev B
Sheet 1 of 4
7-A2-1



IEEE / TIMER -- PC ASSY A2

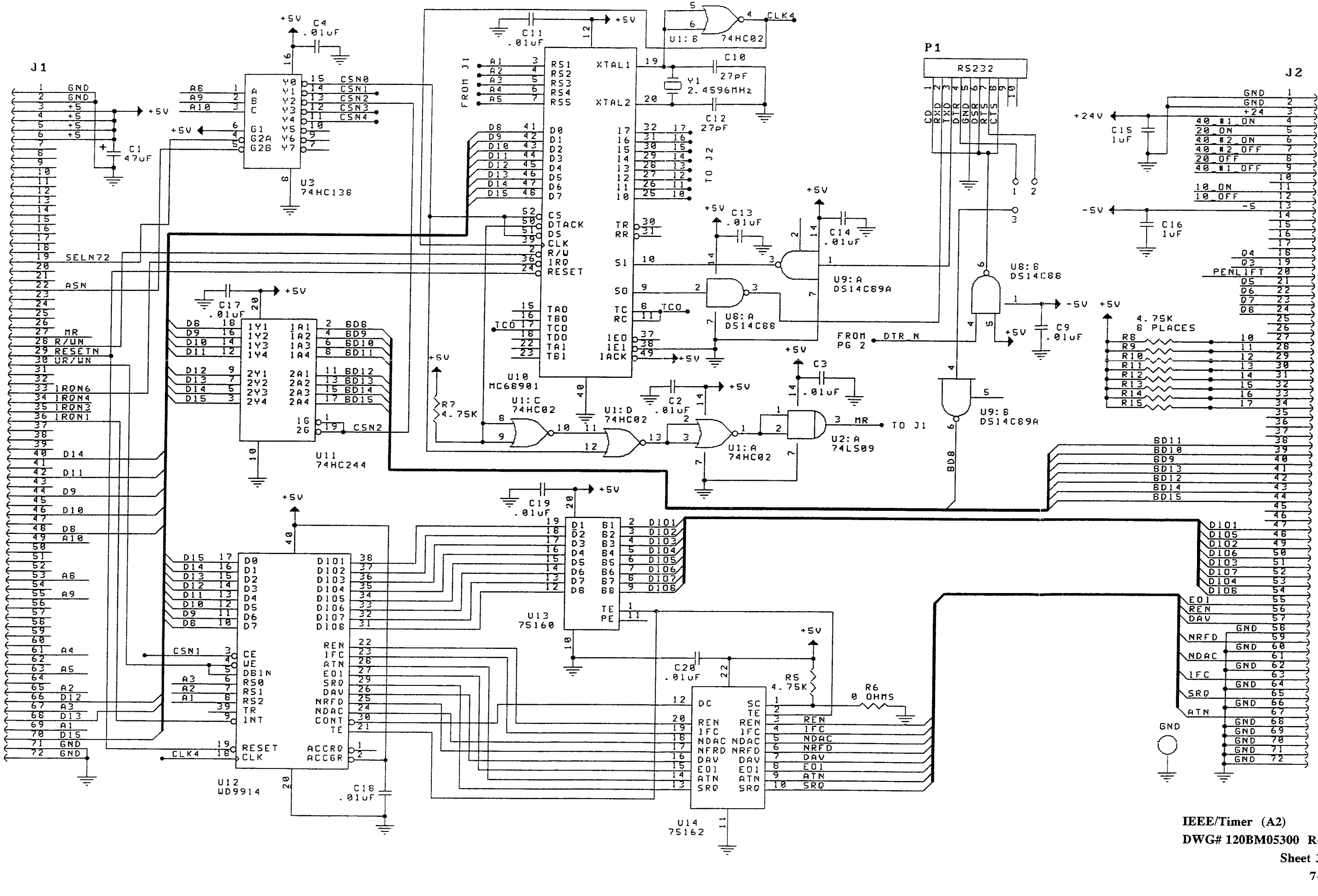
U10 is the interrupt timer for the CPU. It is clocked by the oscillator consisting of Y1, C10, and C12.

U8 and U9 provide for the addition of an RS-232 interface feature which is not yet implemented.

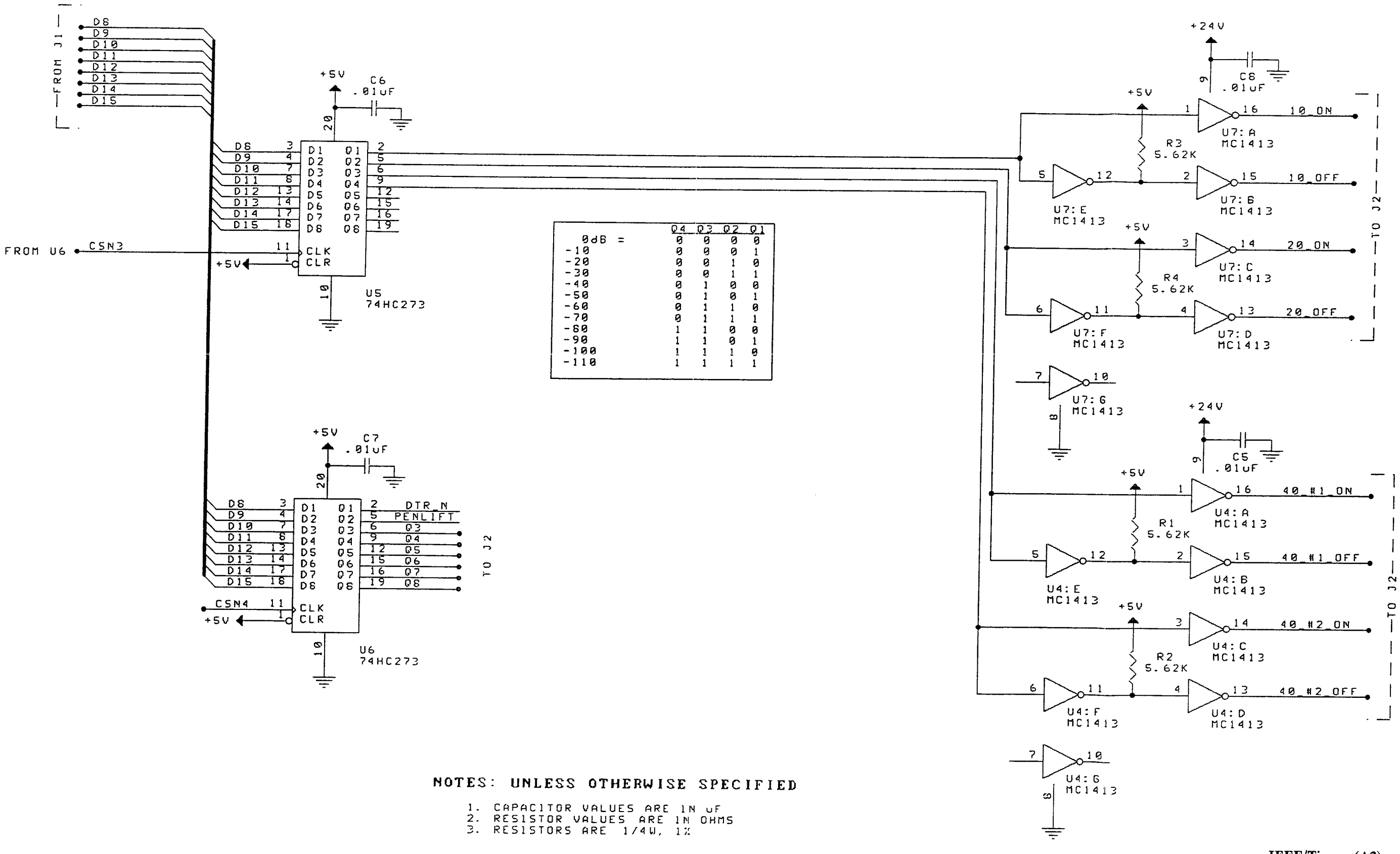
U12, U13, and U14 operate the instrument's remote control interface, which conforms to the IEEE-488 standard.

U3 decodes chip selects for the circuits on this board. U11 acts as a buffer for certain computer bus lines.

On sheet 4, the outputs of flip-flop U5 are used to latch attenuator data; U7 and U4 provide the proper logic levels for driving the attenuator. The outputs of flip flop U6 are used to latch miscellaneous computer control lines.

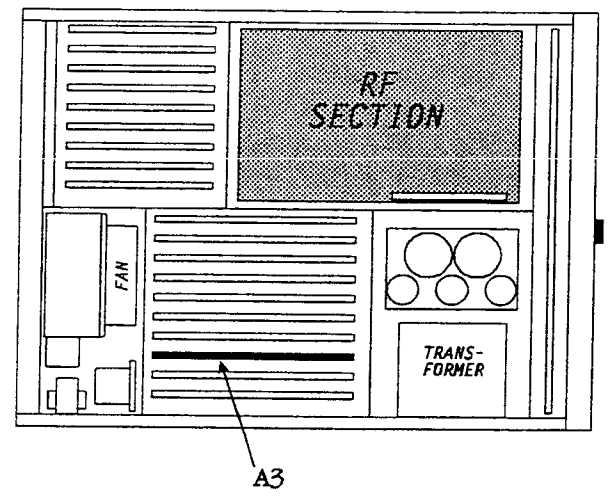


IEEE/Timer (A2)
DWG# 120BM05300 Rev B
Sheet 3 of 4
7-A2-3

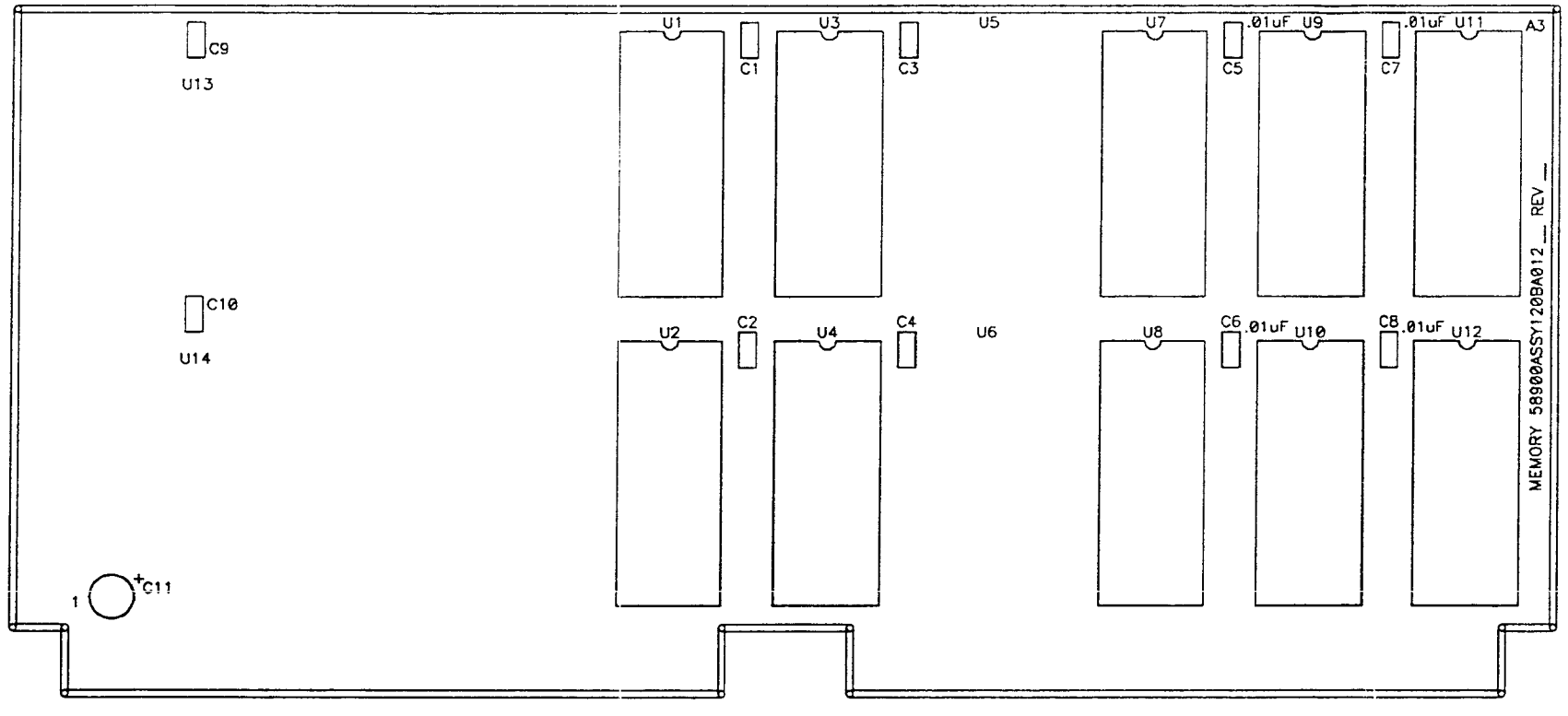


NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/4W, 1%



Memory (A3)
DWG# 120BM01200 Rev C
Sheet 1 of 3
7-A3-1



MEMORY -- PC ASSY A3

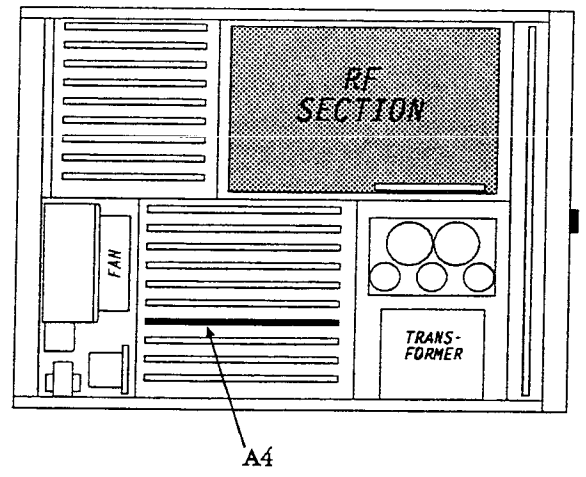
U1 thru U4 are RAMS, used by the CPU for temporary data storage.

U5 thru U14 are ROMs, used to store the instrument's operational software.

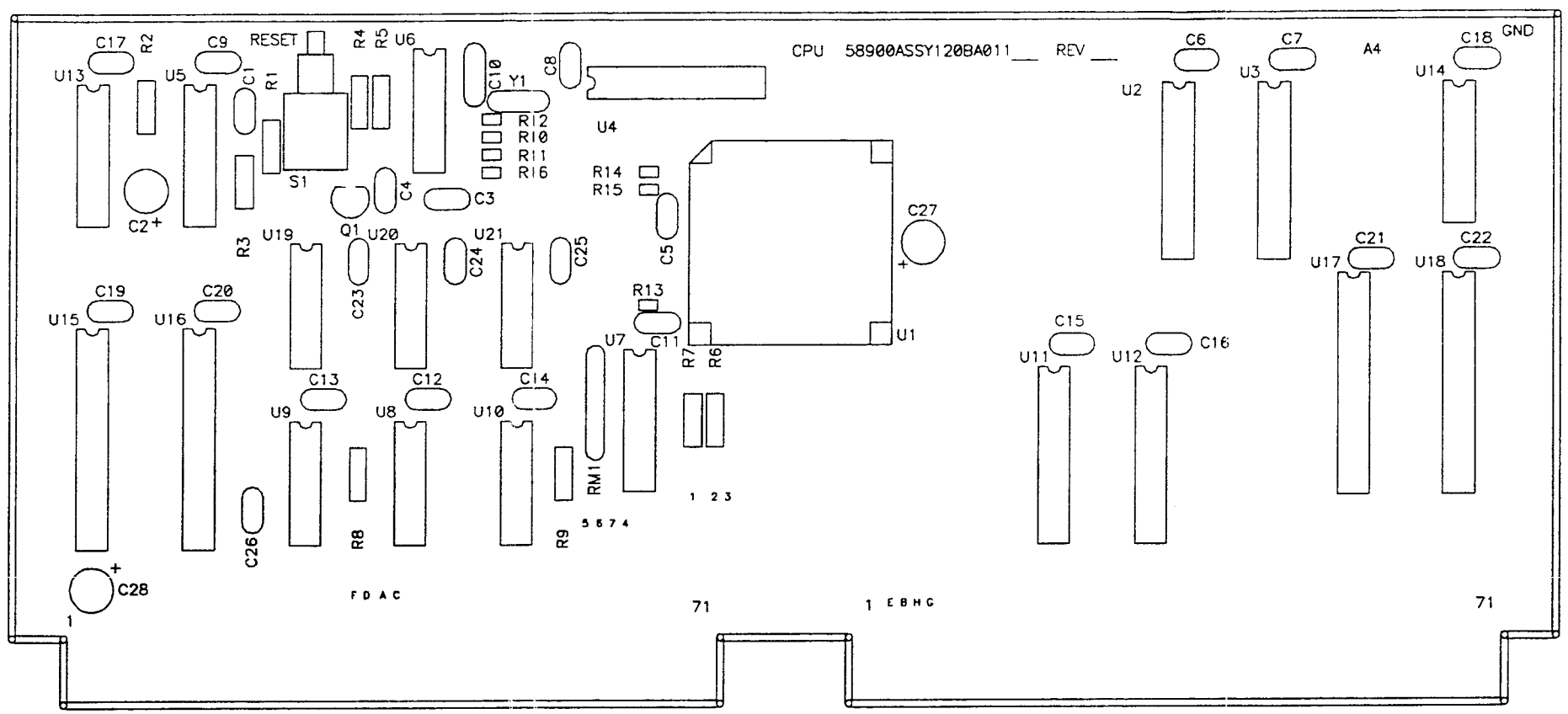
The RAMS and ROMs are 32K X 8 and are used in pairs (one for even addresses and the other used for odd), in order to simulate 32K X 16's as required by the 16 bit data bus.

U1 MCM60256
U2 MCM60256
U3 MCM60256
U4 MCM60256
U5 27C256
U6 27C256
U7 27C256
U8 27C256
U9 27C256
U10 27C256
U11 27C256
U12 27C256
U13 27C256
U14 27C256
C1 .01uF
C2 .01uF
C3 .01uF
C4 .01uF
C5 .01uF
C6 .01uF
C7 .01uF
C8 .01uF
C9 .01uF
C10 .01uF
C11 47uF
+5V
SELN0C
SELN01
LR/UN
SELN0B
SELN_00
SELN0D
UR/UN
SELN0E
SELN00/0F
J1

Memory (A3)
DWG# 120BM01200 Rev C
Sheet 3 of 3
7-A3-3



CPU (A4)
DWG# 120BM01100 Rev C
Sheet 1 of 4
7-A4-1



CPU -- PC ASSY A4

Y1, C3, C4, Q1 and U6 A provide the clock for U1, the 68000 microprocessor chip.

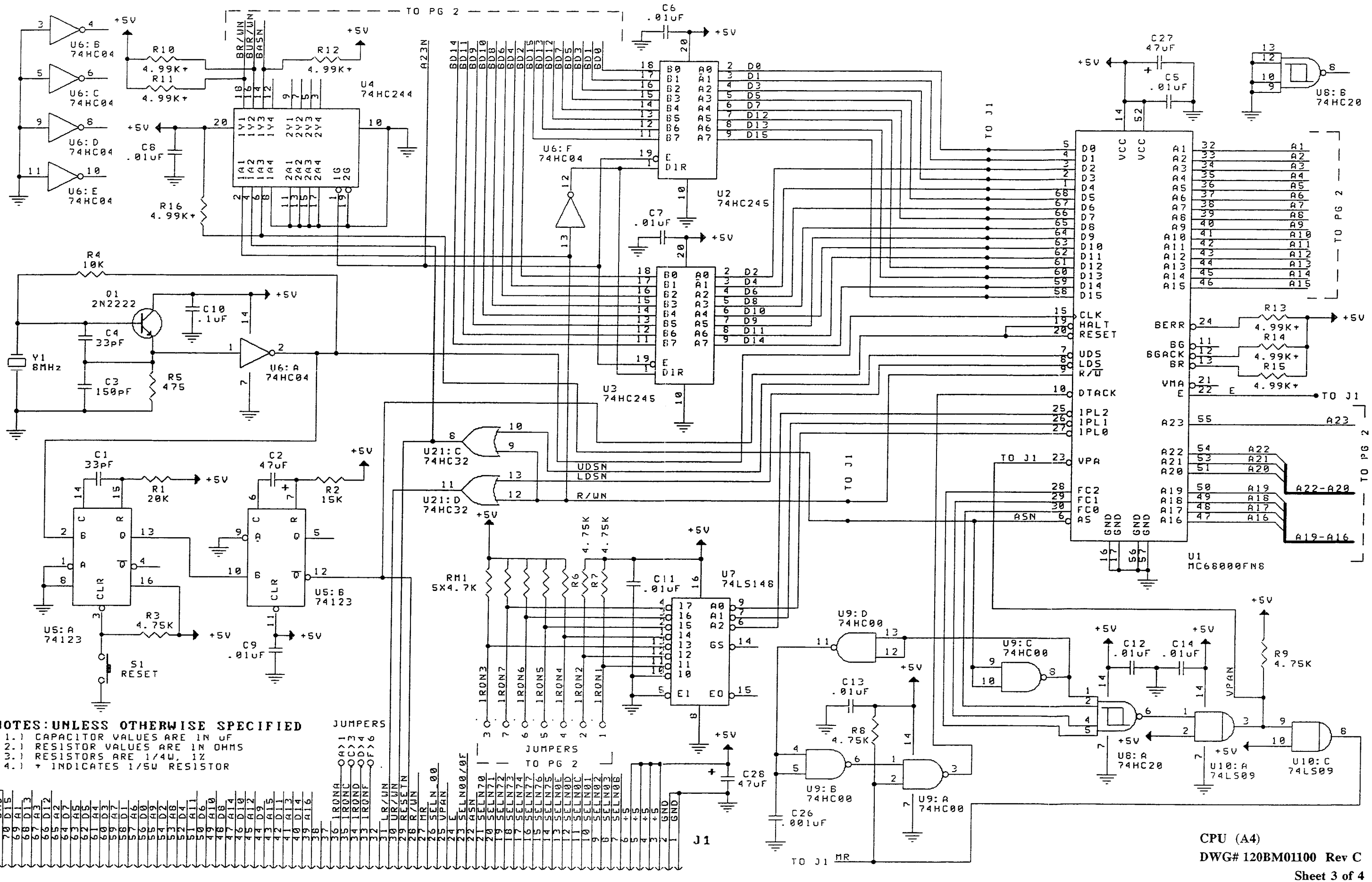
U2, 3 and 4 buffer the output to the I/O data bus.

U5 A and B make up the power on reset logic. The presence of the clock is detected at pin 2. There is a set delay before the reset line switches to prevent failures during brownout or power glitch conditions.

U7 decodes interrupts. When the CPU receives an interrupt, one of the FC0 - FC2 lines is activated causing U8, 9 and 10 to generate several different logic signals. VPAN puts the CPU into the non-vectored interrupt mode in order to handle the interrupt. The MR (memory ready) logic is also generated, which slows the CPU for read/write cycles.

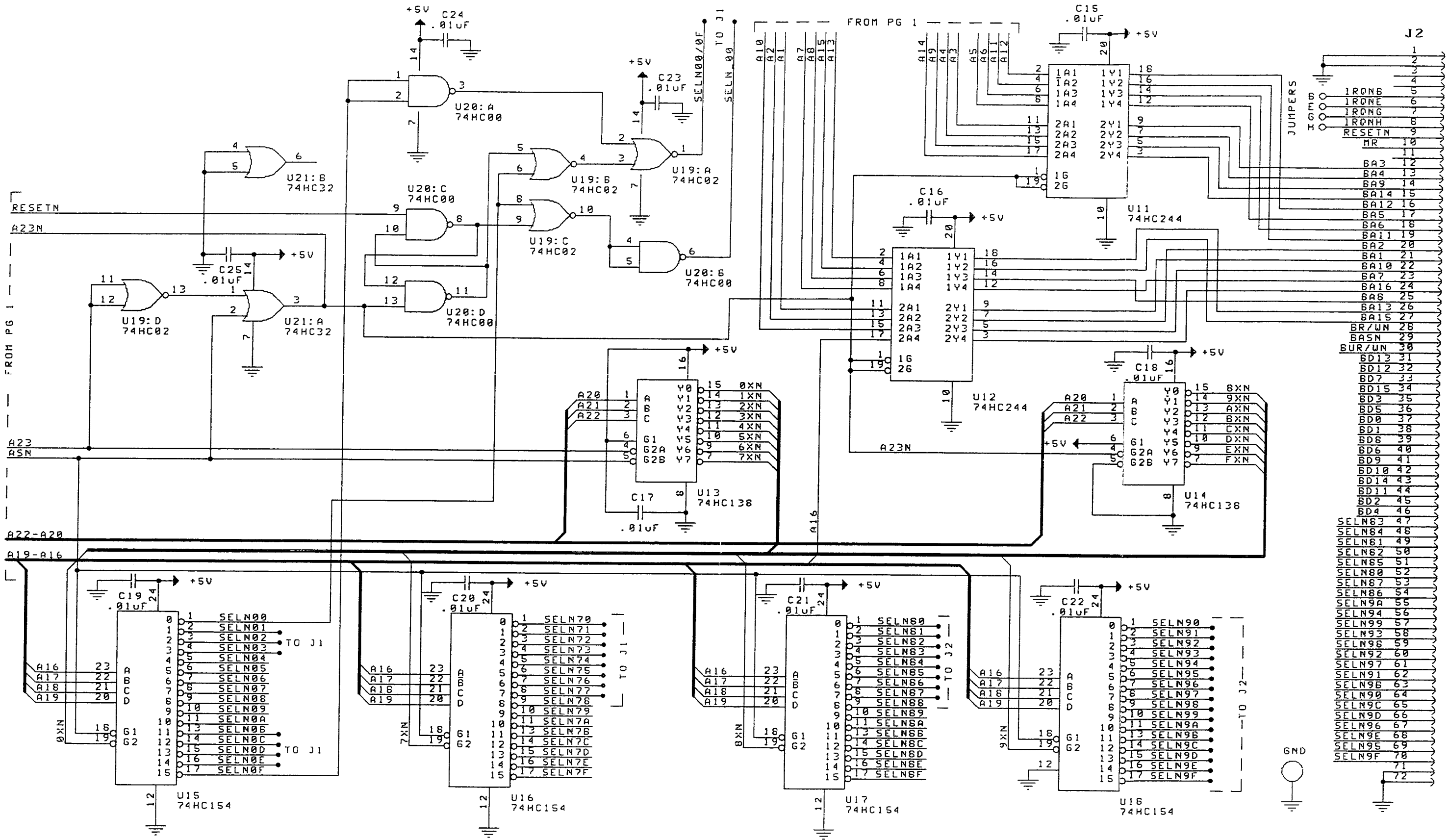
U11 and 12 serve to buffer between the I/O bus and the CPU.

On sheet 4, U13, 14, 15, 16, 17 and 18 decode chip selects for boards or circuits on the I/O bus. U19, 20 and 21 give a startup vector to the CPU on power up.



NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/4W, 1%
4. + INDICATES 1/5W RESISTOR



CPU (A4)
DWG# 120BM01100 Rev C
Sheet 4 of 4
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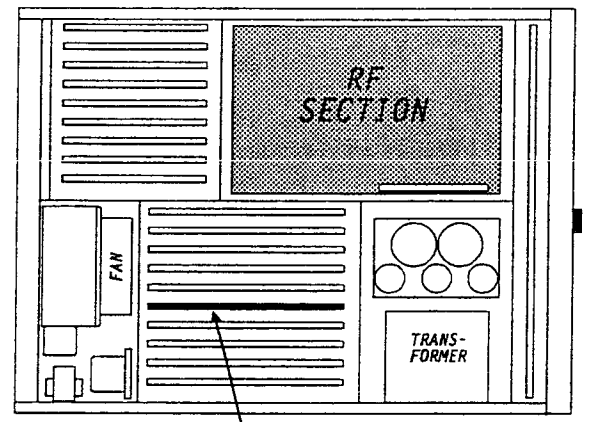
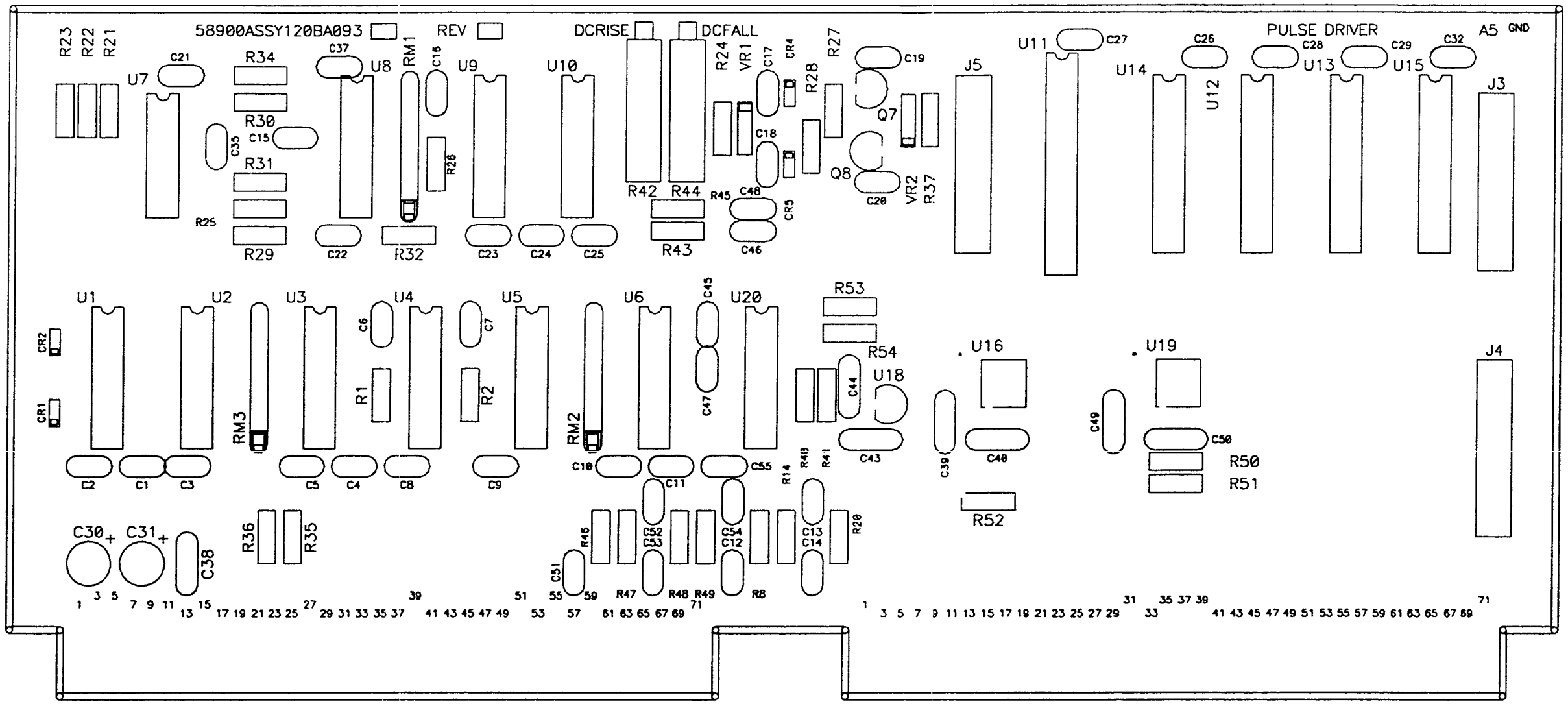


A5, A5A1

Pulse Driver (A5)
DWG# 120BM09302 Rev B
Sheet 1 of 4
7-A5-1



PULSE DRIVER -- PC ASSY A5

The pulse driver PCA has various logic circuits required for directing the pulse signals to the proper locations, as well as the actual pulse driver circuitry which drives the pulse modulators. U12, 13, 14 and 15 are latches providing interface between the I/O bus and the individual circuits on the driver board as well as the pulse generator board (A5A1). U11 decodes the chip selects for the latches and other circuitry.

When EXT Pulse Modulation is selected, the external pulse signal is received at PM_IN, U1-5. The external signal and its complement are output on U1-2 and U1-4. EPM- logic at U1-7 selects one of the signals to propagate U2 A or B, selecting + or - edge trigger when EXT TRIG (+ or -) or EXT PULS (+ or -) is selected. In the case of EXT TRIG the trigger signal (TRIGN) is supplied to the pulse generator PCA (A5A1) via U4 D, U8 C and U9 C. The external pulse signal from U2 A or B is allowed to propagate thru U2 D and ultimately on to the pulse drivers, when U2 D is enabled via U3 A and the EXTPUL logic signal.

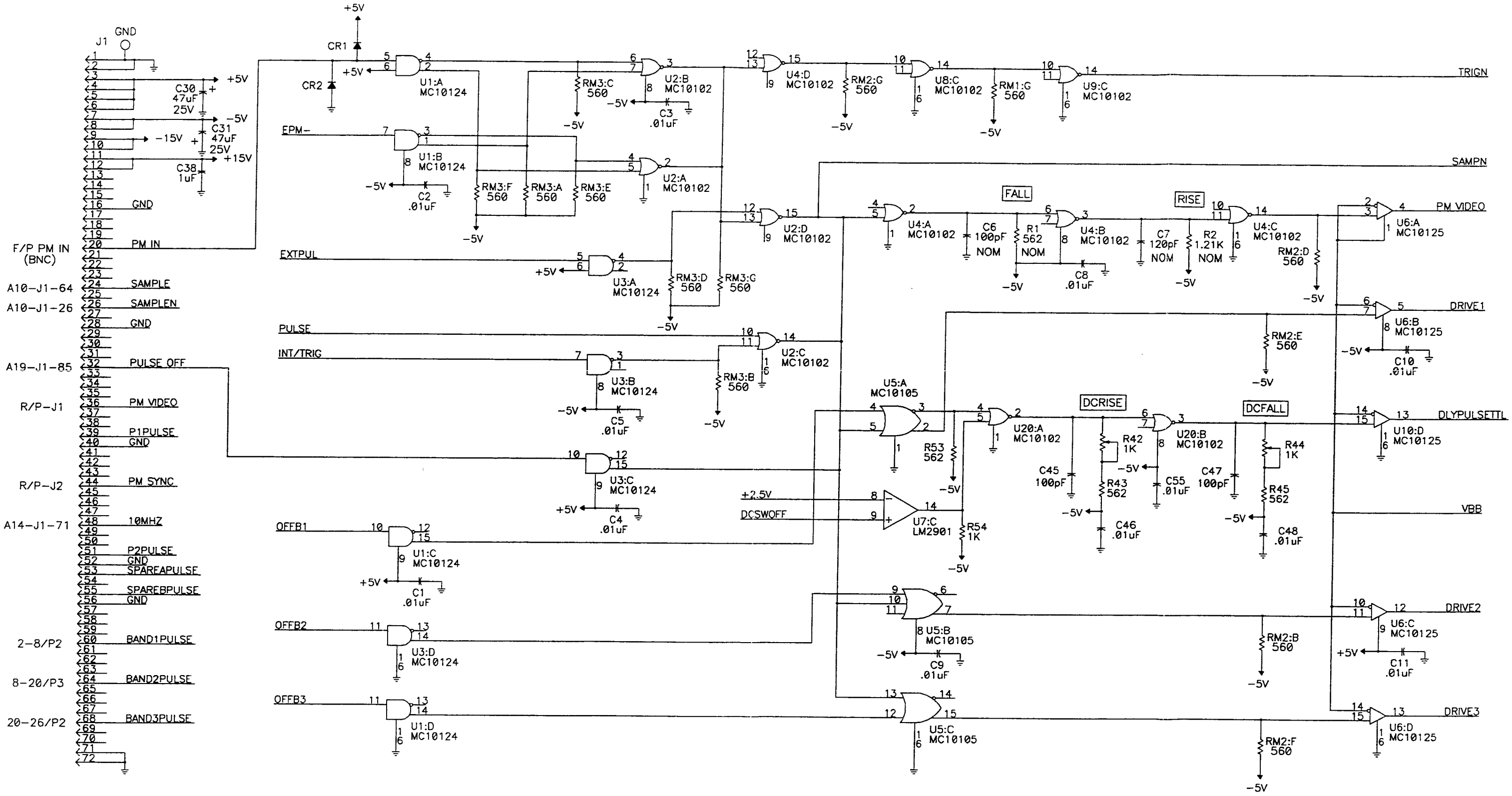
The PULSE signal from the pulse generator PCA is allowed to propagate thru U2 C and ultimately on to the pulse driver circuitry, when the INT/TRIG signal is true. This allows only one signal at a time, either the external pulse signal or the internal pulse signal, to drive the pulse modulators.

The selected pulse signal is provided to the rear panel as the PM_VIDEO signal after being translated to a TTL signal.

U6 A, U4 and associated components allow the rising and falling edge of this signal to be positioned to align with the actual pulsed RF out of the unit. In addition the selected pulse signal (referred to as SAMPN on the schematic) is used for the purpose of sampling the detector voltage on the leveling board when the RF is on. In order to do this it is necessary to delay and shorten the pulse. This is done by U8 A, B, D, U9 A, B and D. The signal is then translated by U10 A, B, Q7 and Q8 to signal levels which are capable of switching the FET samplers on the Leveling PCA. The resulting signal is called SAMPLE.

U1 C and D, and U3 D handle the logic which selects the proper driver to be enabled at U5 A, B or C. The pulse signal is translated to TTL levels at U6 B thru D.

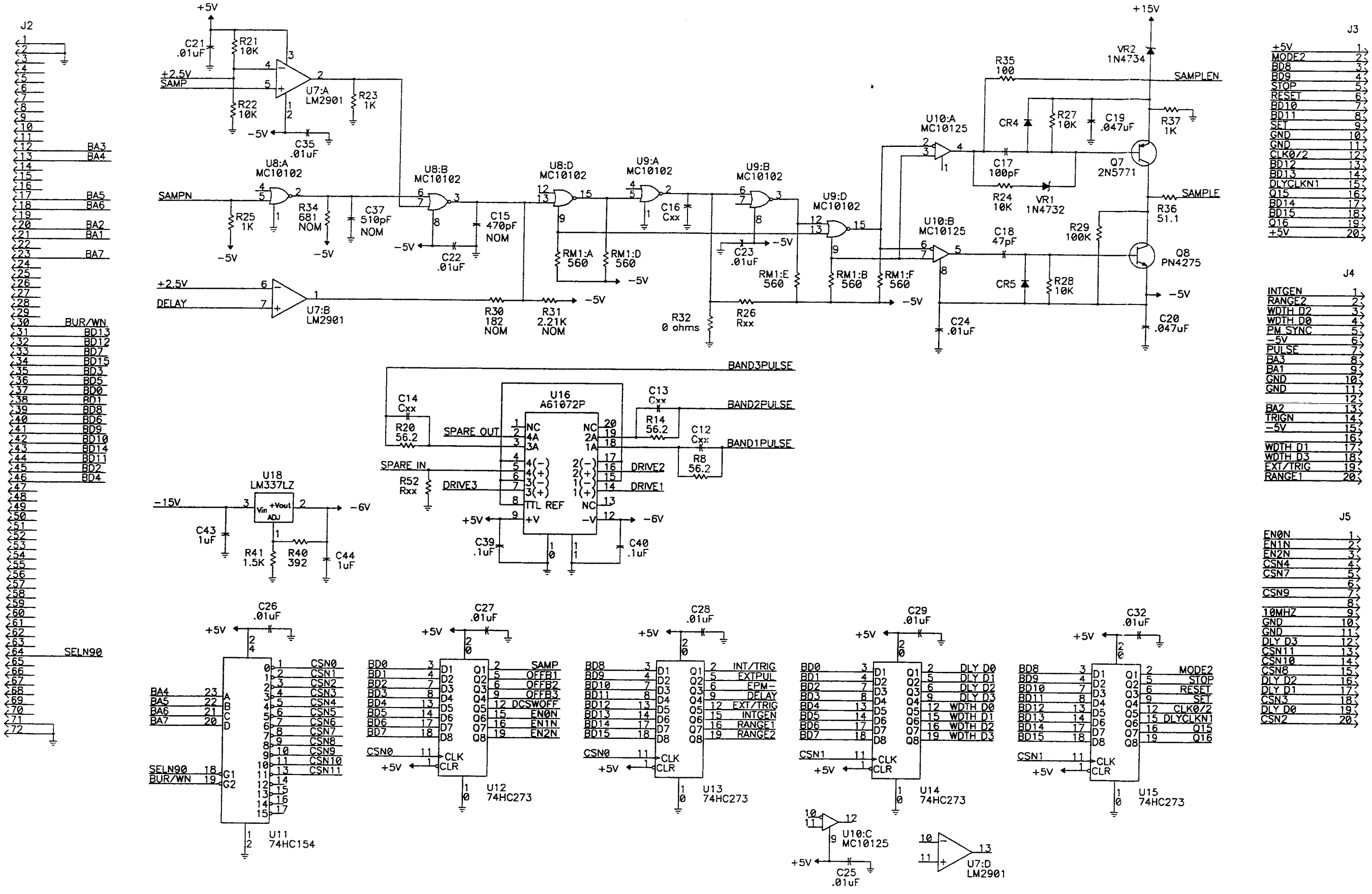
When pulse modulation is not selected the FET samplers on the leveling PCA must stay on continuously. The PULSE_OFF logic signal serves this purpose via U3 C and U7 A.



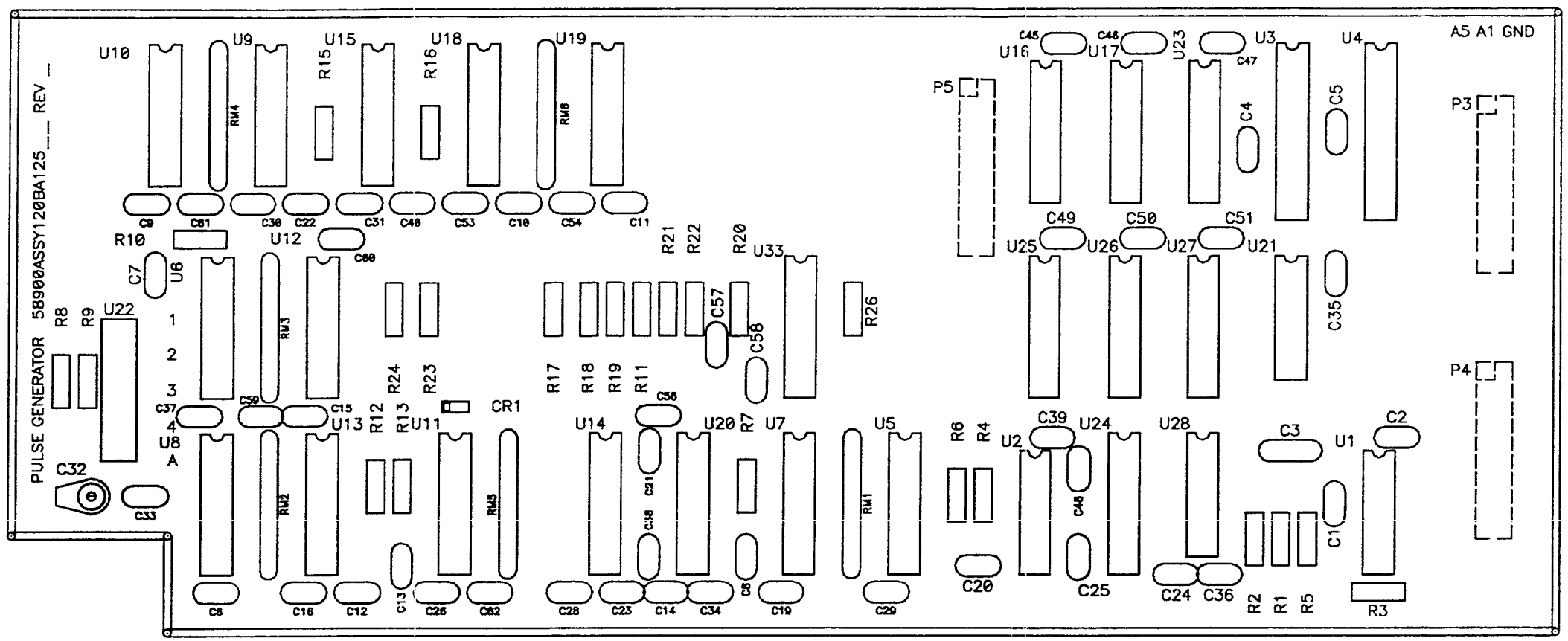
NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN uF.
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/4W, 1%
4. DIODES ARE 1N4148

Pulse Driver (A5)
DWG# 120BM09302 Rev B
Sheet 3 of 4
7-A5-3



Pulse Driver (A5)
DWG# 120BM09302 Rev B
Sheet 4 of 4
7-A5-4



PULSE GENERATOR -- PC ASSY A5A1

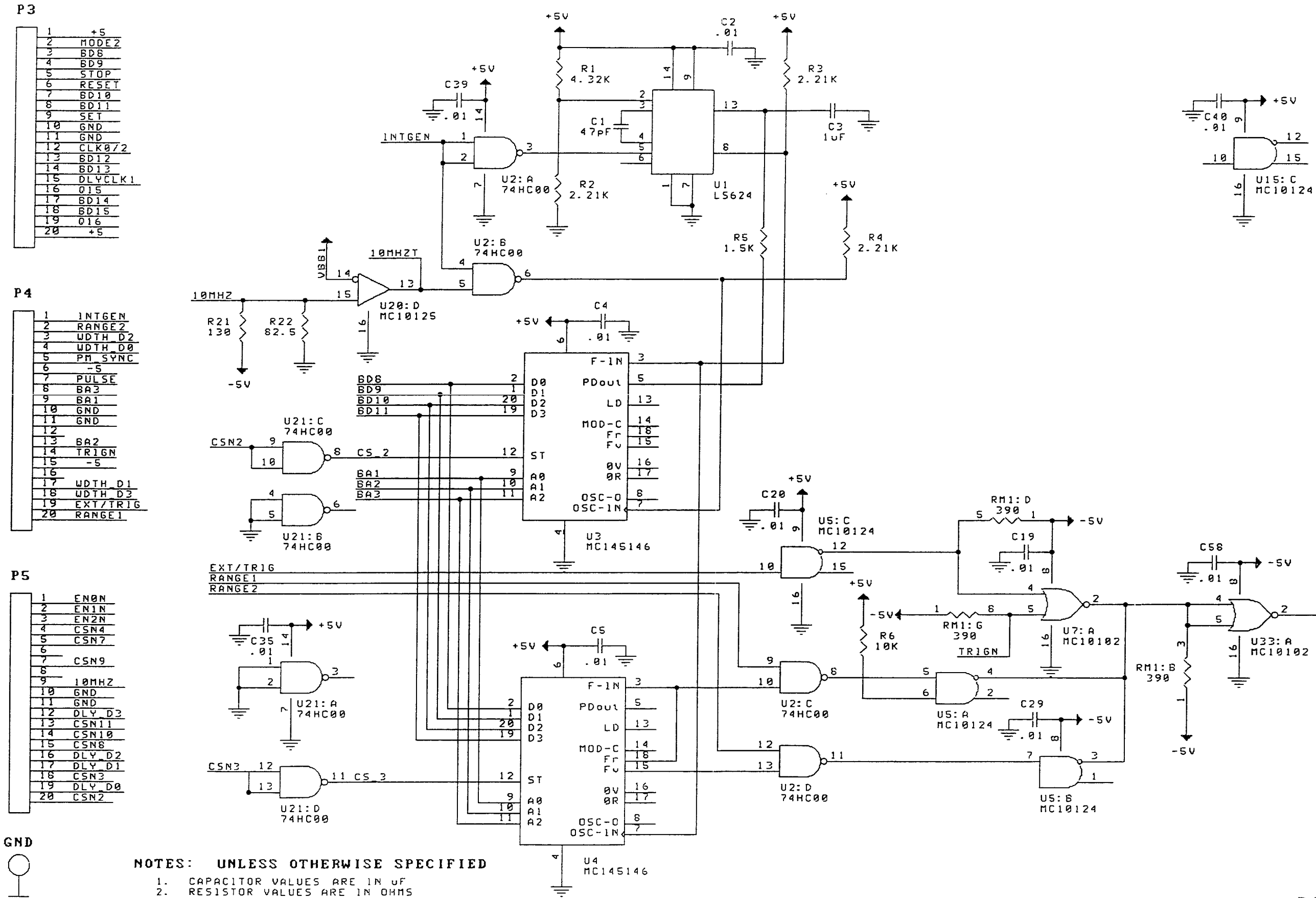
The pulse generator is, as its name implies, a generator. The generator can be separated into 3 sections: the Rate generator, the delay circuitry and the width circuitry.

The rate generator is composed of a phase locked loop with a 10 MHz reference which is translated to TTL levels at U20 D and then enabled at U2 B. U1 is a 3 to 10 MHz VCO and the PLL integrated circuit U3 contains the phase comparator and dividers for the loop. The loop output can be divided by another set of dividers in U4, also programmed by the computer, to give additional frequency ranges which can be selected by U2 C or D. The internal rate generator can be overridden by an external pulse signal or external trigger signal from U5 C. The selected internal or external signal propagates thru U33 A; this is the STARTN signal which is used to gate (via U6 A) a 100 MHz delay line clock U8 D, U22 and C32 and C33. This signal is turned into a PM_SYNC signal by U33 D, C, U7 B, C and U20 C, for output to the rear panel.

The delay is generated in 10 ns increments by multiple counters which are clocked by the 100 MHz clock described above. The first counter U10 is a 4 bit counter which counts delays up to 160 ns, U16 a 8 bit counter counts up to approximately 40.9 us in 160 ns increments, U17 counts up to approximately 10.485 ms in 40.9 us increments and U23 counts up to approximately 2.6 s in 10.485 us increments. These counters are programmed by the computer, allowing up to 2 seconds of delay programmable in 10 ns increments. When the delay cycle is completed and the DEND from U28 A and the COUT from U10 have propagated thru the gates giving low inputs at U8-6 and 7, U6-10 is toggled and the width cycle starts on the next clock cycle. The beginning of the width cycle causes U6-15 to go high, this signal, after propagating thru U13 A and U33 B, is the actual pulse signal which will ultimately drive the RF pulse modulators.

The width is also generated in 10 ns increments and the counters (U11, U25, U26 and U27) are set up similarly to those which control the delay cycles. The width cycle ends when both inputs to U8 C are low (this is controlled by U11 COUT and U28 DEND), causing U6 to be reset.

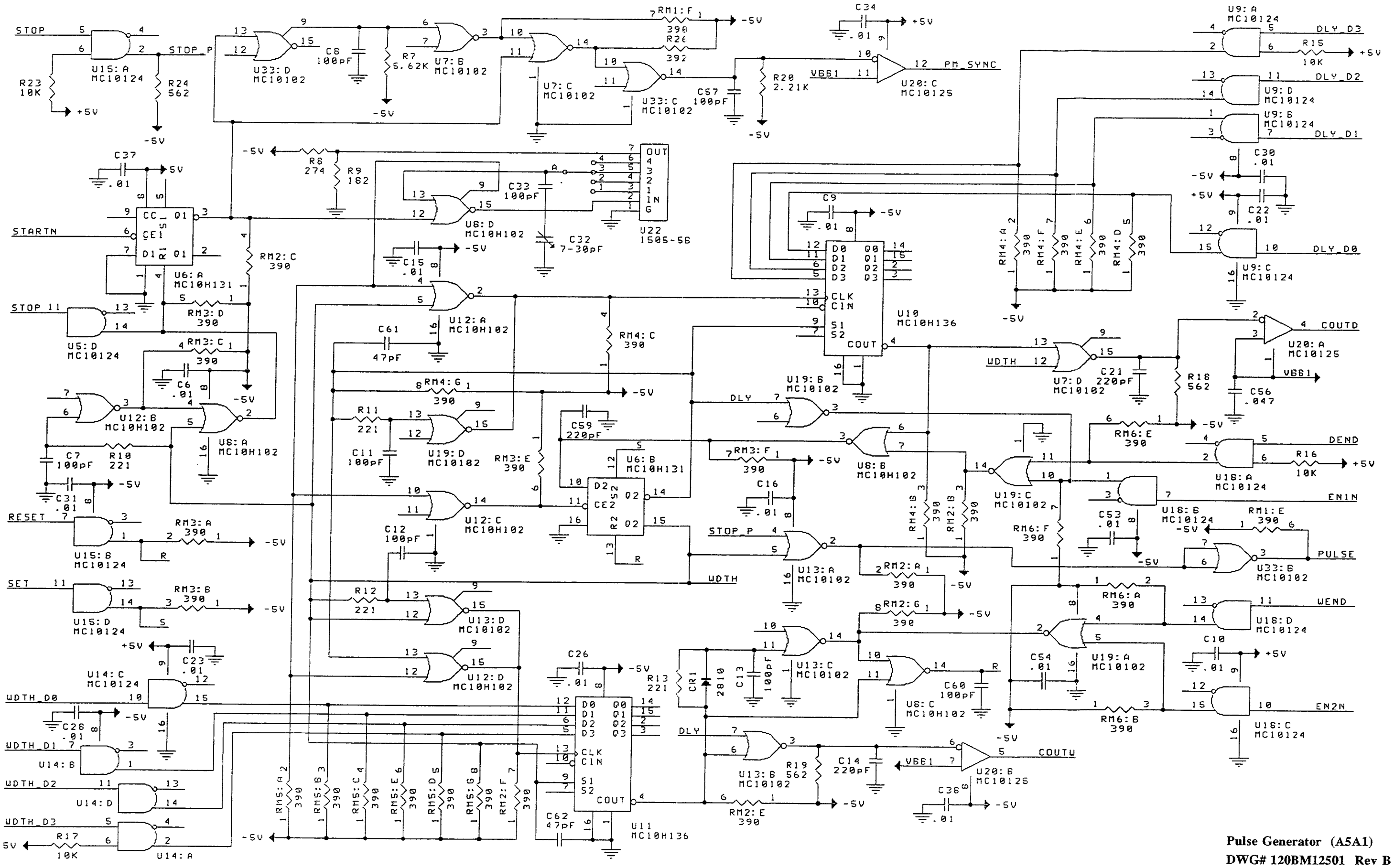
The next trigger from the rate generator will start another delay and width cycle.



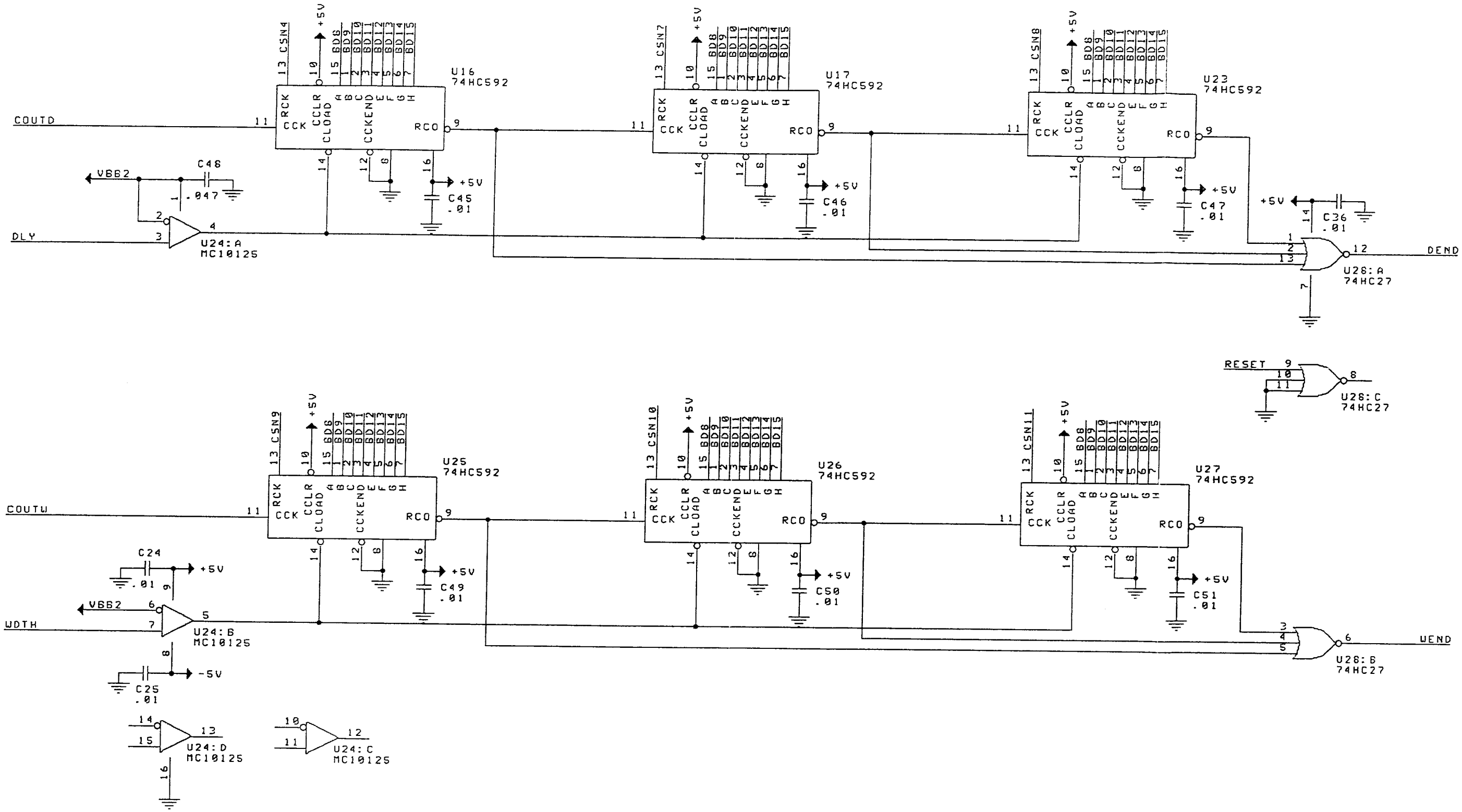
NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/4W, 1%
4. RESISTOR PACKS ARE 7x390 OHMS

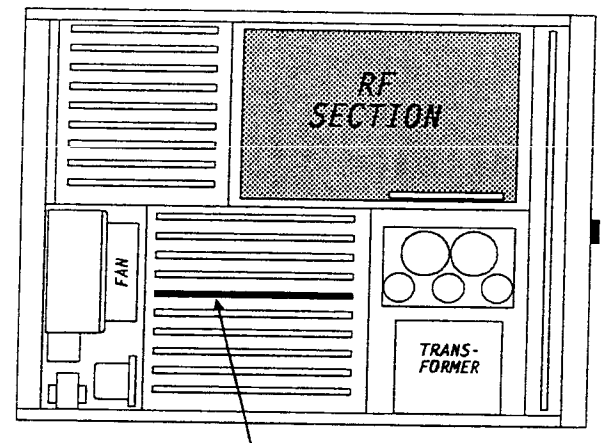
Pulse Generator (A5A1)
DWG# 120BM12501 Rev B
Sheet 2 of 4
7-A5-6



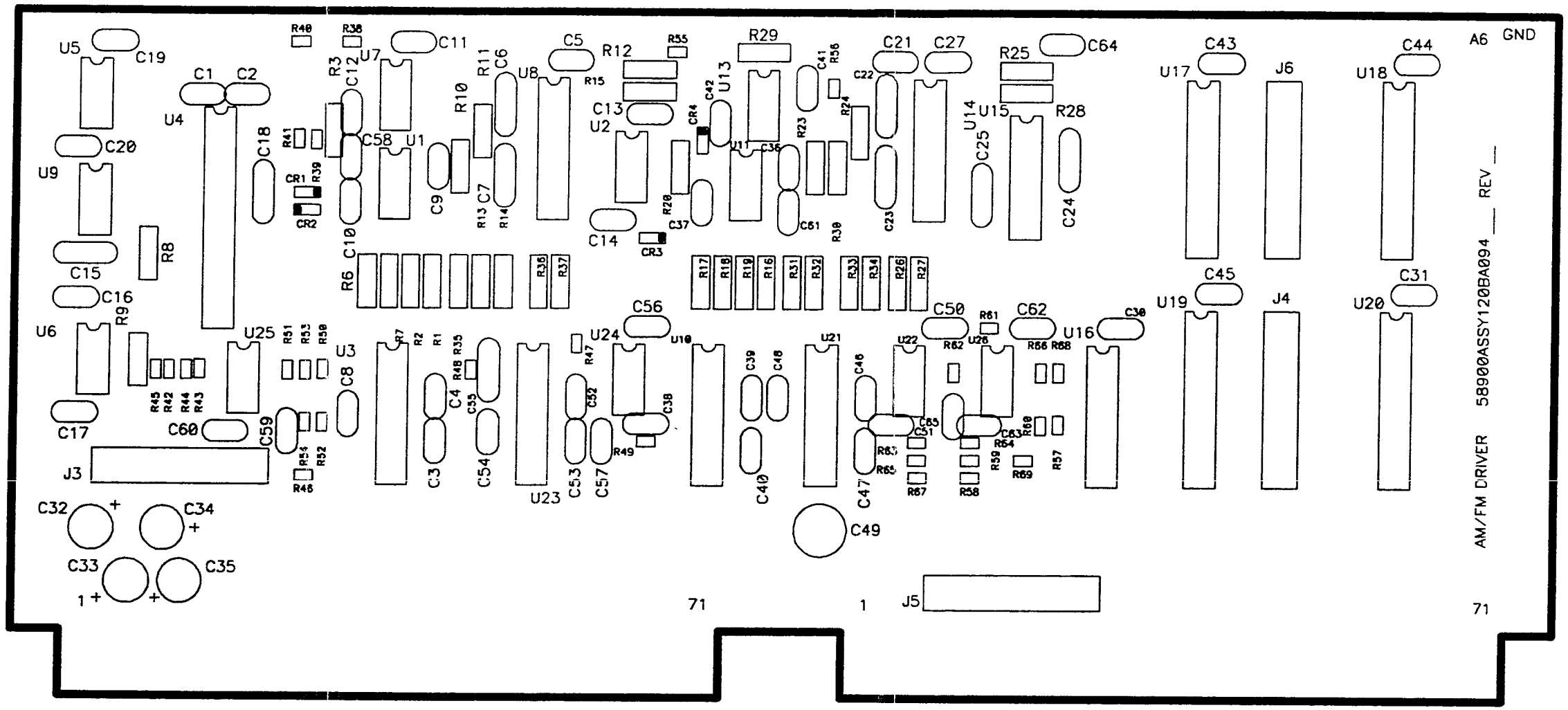
Pulse Generator (A5A1)
DWG# 120BM12501 Rev B
Sheet 3 of 4
7-A5-7



Pulse Generator (A5A1)
DWG# 120BM12501 Rev B
Sheet 4 of 4
7-A5-8



A6, A6A1



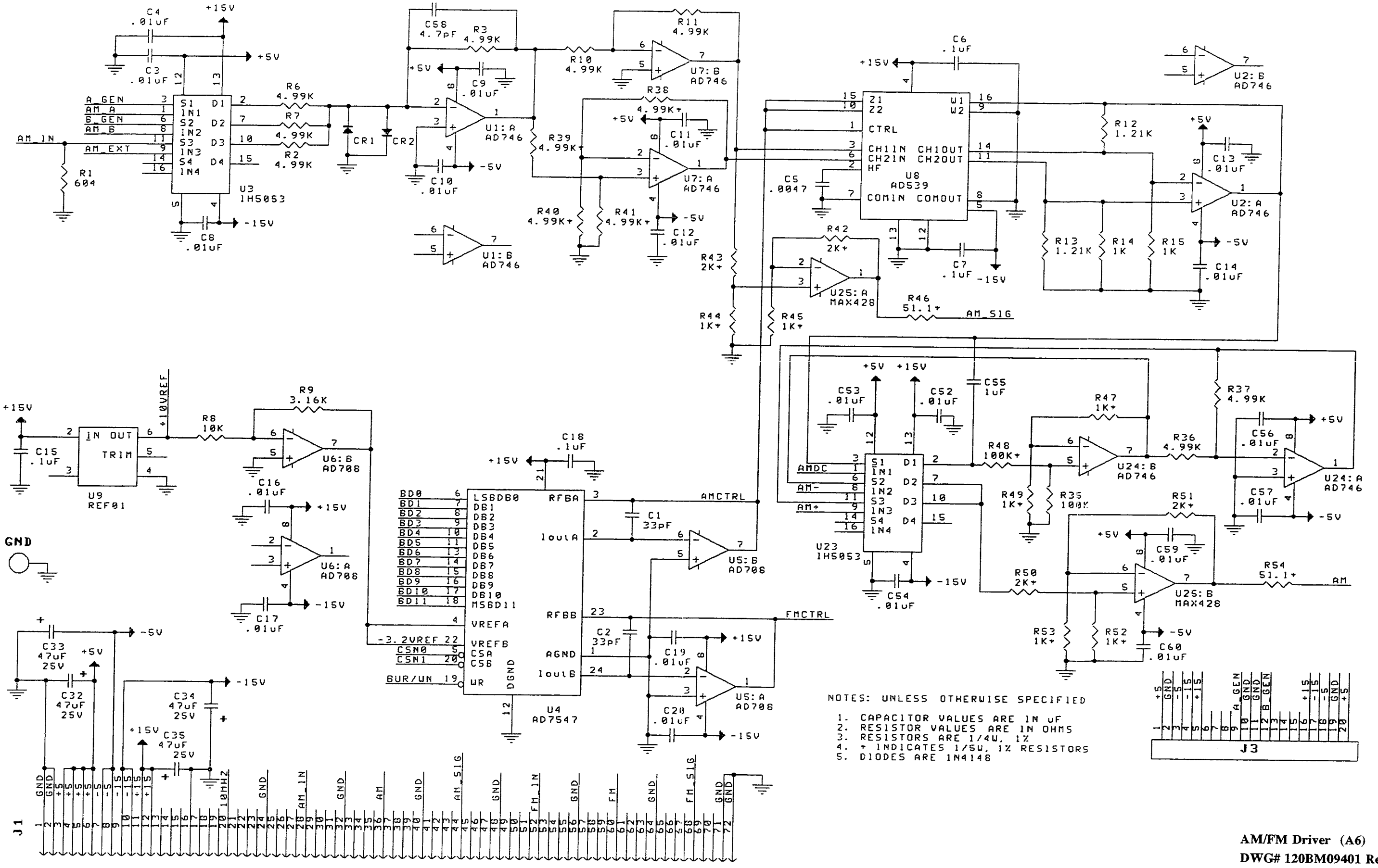
AM/FM DRIVER -- PC ASSY A6

The AM/FM driver PCA has two main functions. The first is to select the internal or external AM or FM signal. The second is to adjust the amplitude of the selected signal according to the depth or deviation required before outputting the signal to the level board (for AM) or the output PLL (for FM).

U3 is an analog switch which is used to select the external AM signal or a signal from the internal generator. The selected signal is buffered by U1 and then converted to a differential signal by U7 A and B. One side of this differential signal is buffered by U25 A for output to the rear panel as the AM_SIG output. Modulator IC, U8, functions as a variable attenuator which is controlled by a voltage from the DAC U4. The voltage at U5-7 changes according to the selected AM depth of modulation. The DAC has a reference voltage which is derived from U9, inverted and attenuated to give 3.2 volts. The output of the variable attenuator U8 is a differential signal which is combined by U2 A to give a single AM signal output. U23 switches this output (the signal can be switched to be DC coupled or inverted to give an output which is 180 degrees out of phase with the input signal) to the input of U25 B which provides the AM signal to the level board A10.

U10 is an analog switch which is used to select the external FM signal or a signal from the internal generator. The selected signal is buffered by U11 and then converted to a differential signal by U13 A and B. One side of this differential signal is buffered by U26 A for output to the rear panel as the FM_SIG output. The voltage from DAC U4 and U5 A controls the amplitude of the FM signal via U14, depending on the deviation selected. The output of the variable attenuator U14 is a differential signal which is combined by U15 to give a single signal output. This output is then switched by U21 (the signal can be switched to be DC coupled or inverted to give an output which is 180 degrees out of phase with the input signal) to the input of U26 B which provides the FM signal for the output PLL board A18.

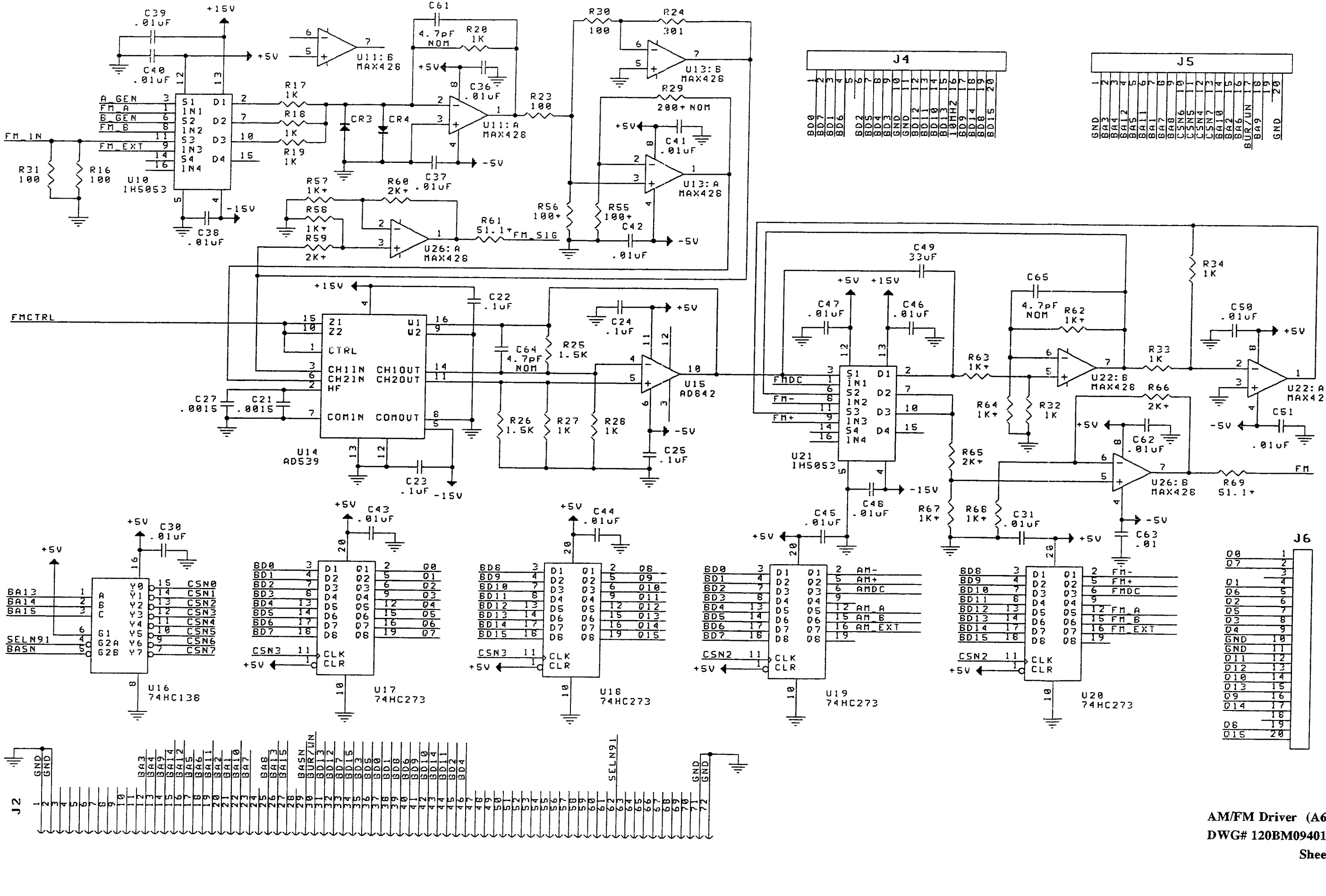
U16 decodes chip select lines for other IC's on the board. U17 thru U20 are required to latch data for circuits on this board and also for circuits on the A6A1 PCA.



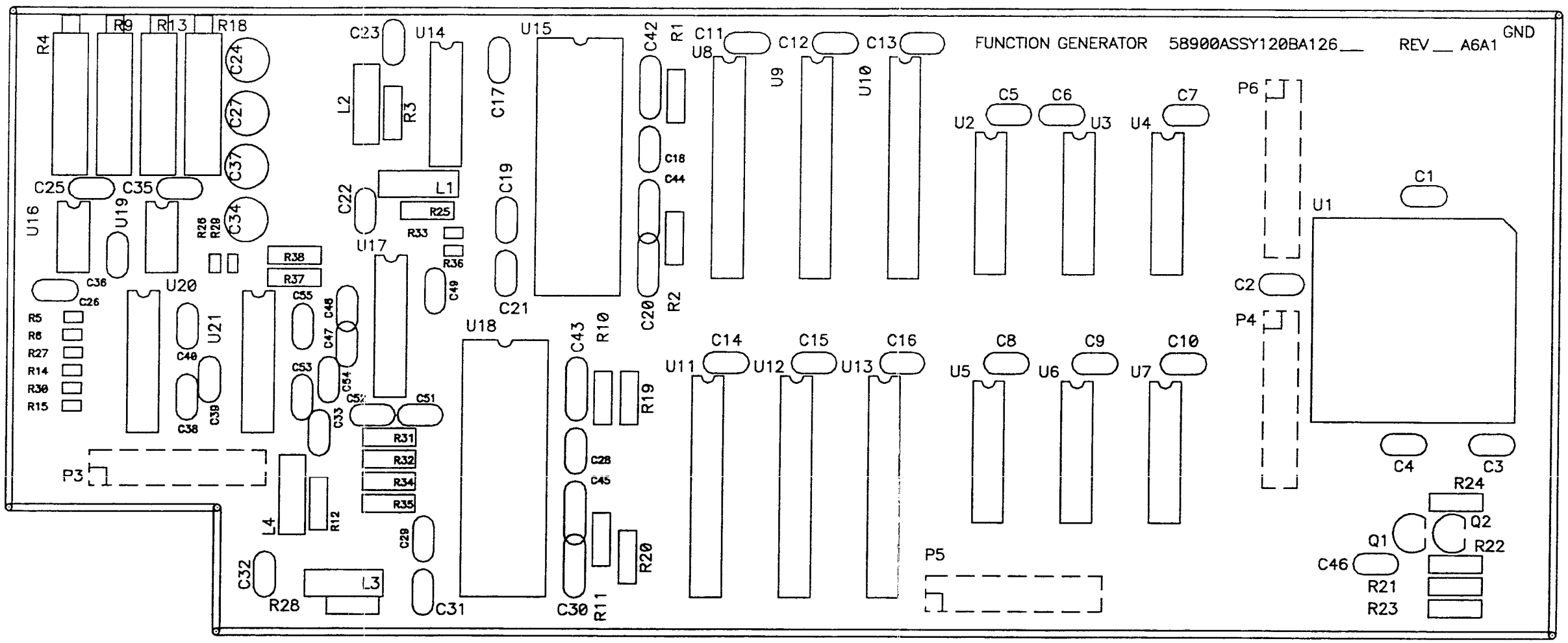
NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/4W, 1%
4. + INDICATES 1/5W, 1% RESISTORS
5. DIODES ARE 1N4148

AM/FM Driver (A6)
DWG# 120BM09401 Rev A
Sheet 3 of 4
7-A6-3



AM/FM Driver (A6)
DWG# 120BM09401 Rev A
Sheet 4 of 4
7-A6-4

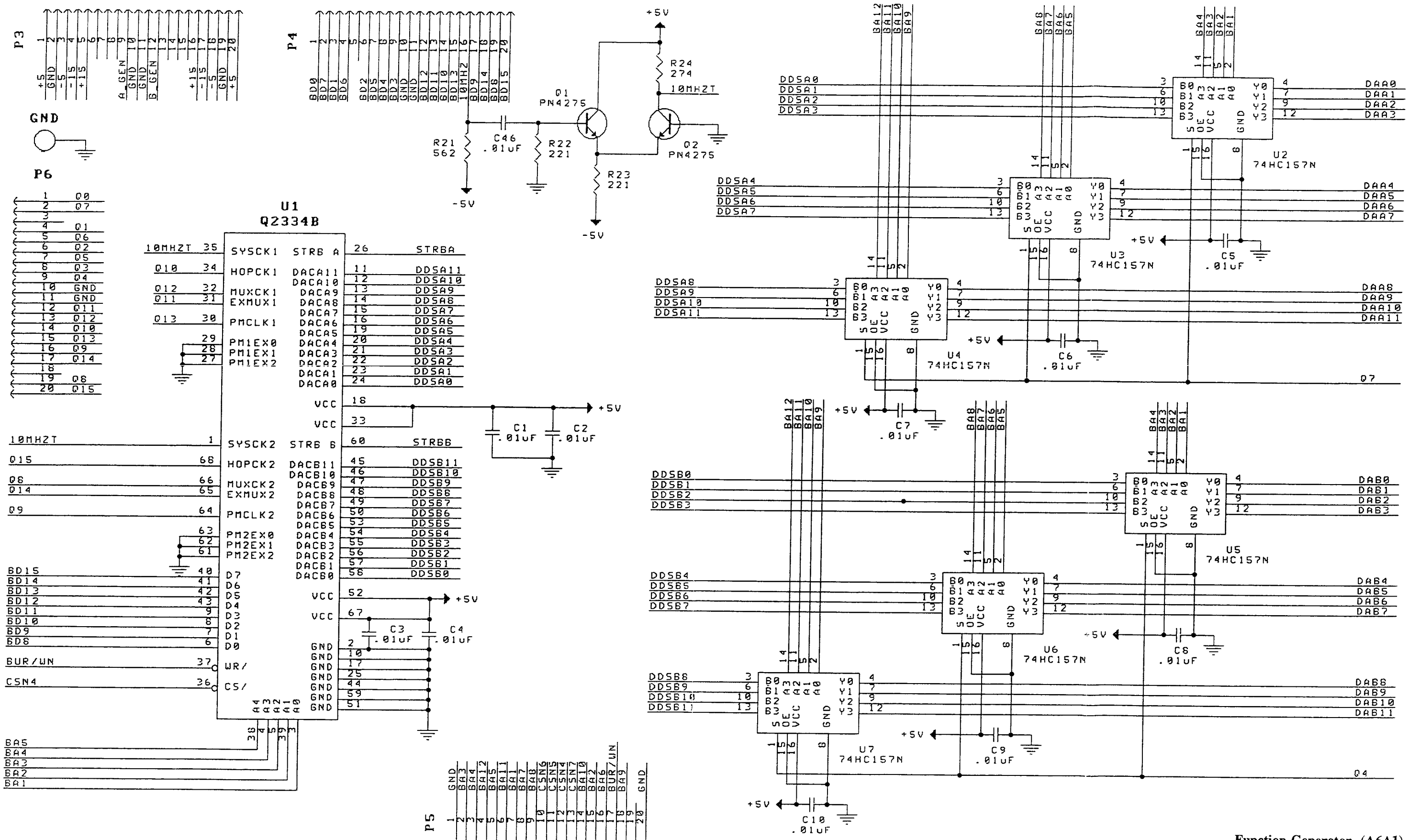


FUNCTION GENERATOR -- PC ASSY A6A1

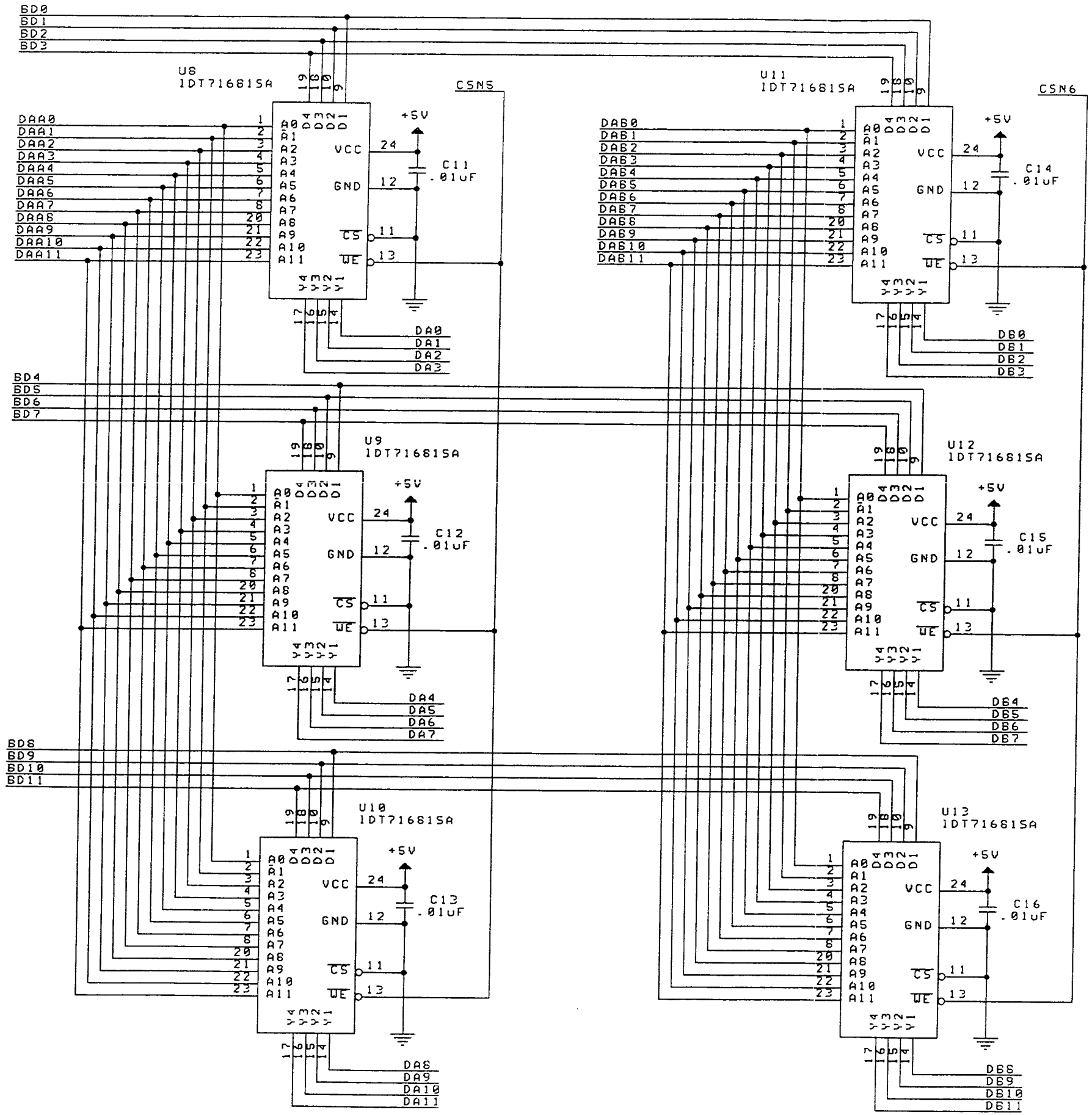
The heart of the Function Generator board is the "Function Generator" chip U1. This IC requires a 10 MHz clock which is supplied external to the board but buffered on board by Q1 and Q2. The IC actually contains two function generators which have been designated as gen A and gen B.

For gen A multiplexers U2, U3 and U4 are used to address RAMs U8, U9 and U10. If INT SINE wave is selected then the computer stores data into the RAMs which is equal to the address which is being programmed. However if INT TRI wave is selected, the computer performs a function on the address data which turns the data from sine data into triangle data and stores the new data into the RAMs. Now a sine or triangle wave is created when the function generator chip outputs data which addresses the RAM and the RAM data becomes DAC U15 input data. The output of this DAC will be the sine or triangle wave (whichever was selected). The components L1, L2, C21, C22, C23 create a low pass filter required to filter out the 10 MHz clock glitches. The SINE CAL pot R4 is used to adjust the amplitude of the sine wave which is then amplified by U16 A the output of which is switched by analog switch U20 or U21. U21 can be switched to allow the sine wave to be converted to a square wave, via U17, the duty cycle of which can be adjusted using R31 and R32. The output of U17 A drives the SQR CAL pot which allows adjustment of the amplitude of the square wave which is then buffered by U16 B before arriving at U20 analog switch. At U20 the Sine or Square wave signal is switched for A_GEN output to the AM/FM Driver PCA (A6).

Generator B operates identically to generator A and has its own set of multiplexers U5, U6 and U7, RAM's U11, U12, U13, DAC U18 and sine wave to square wave converter U17 D.

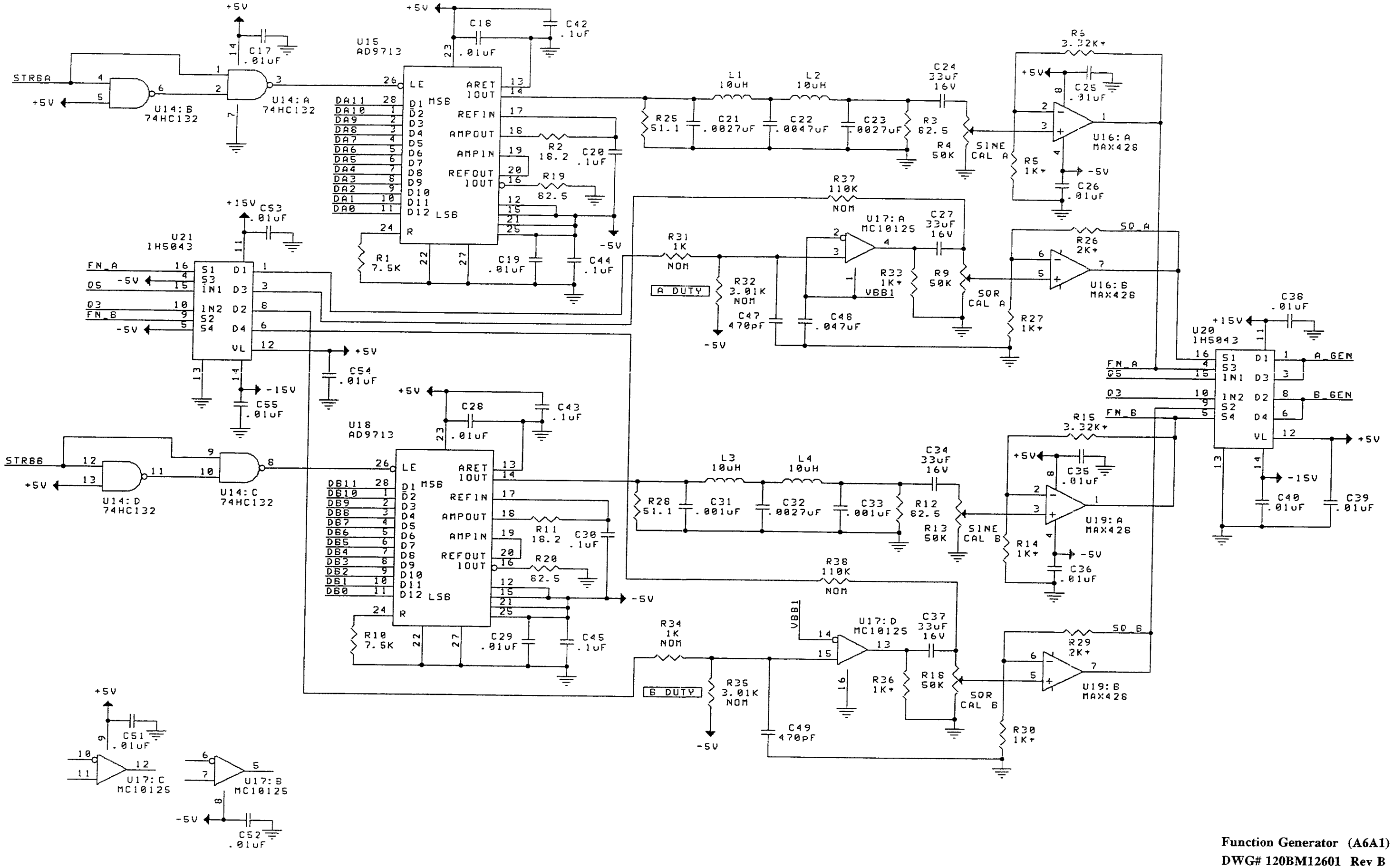


Function Generator (A6A1)
DWG# 120BM12601 Rev B
Sheet 2 of 4
7-A6-6

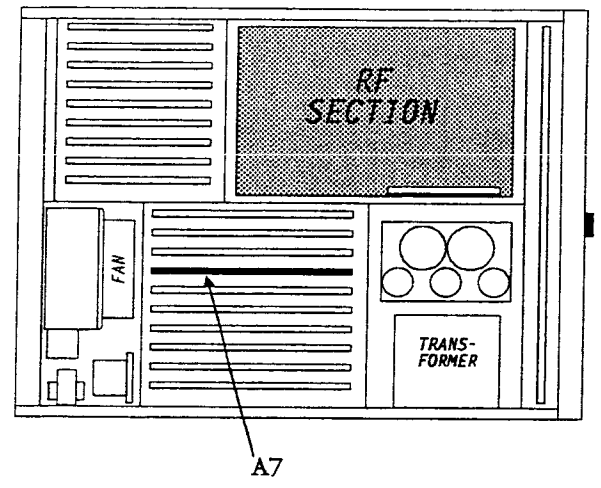


NOTES: UNLESS OTHERWISE SPECIFIED

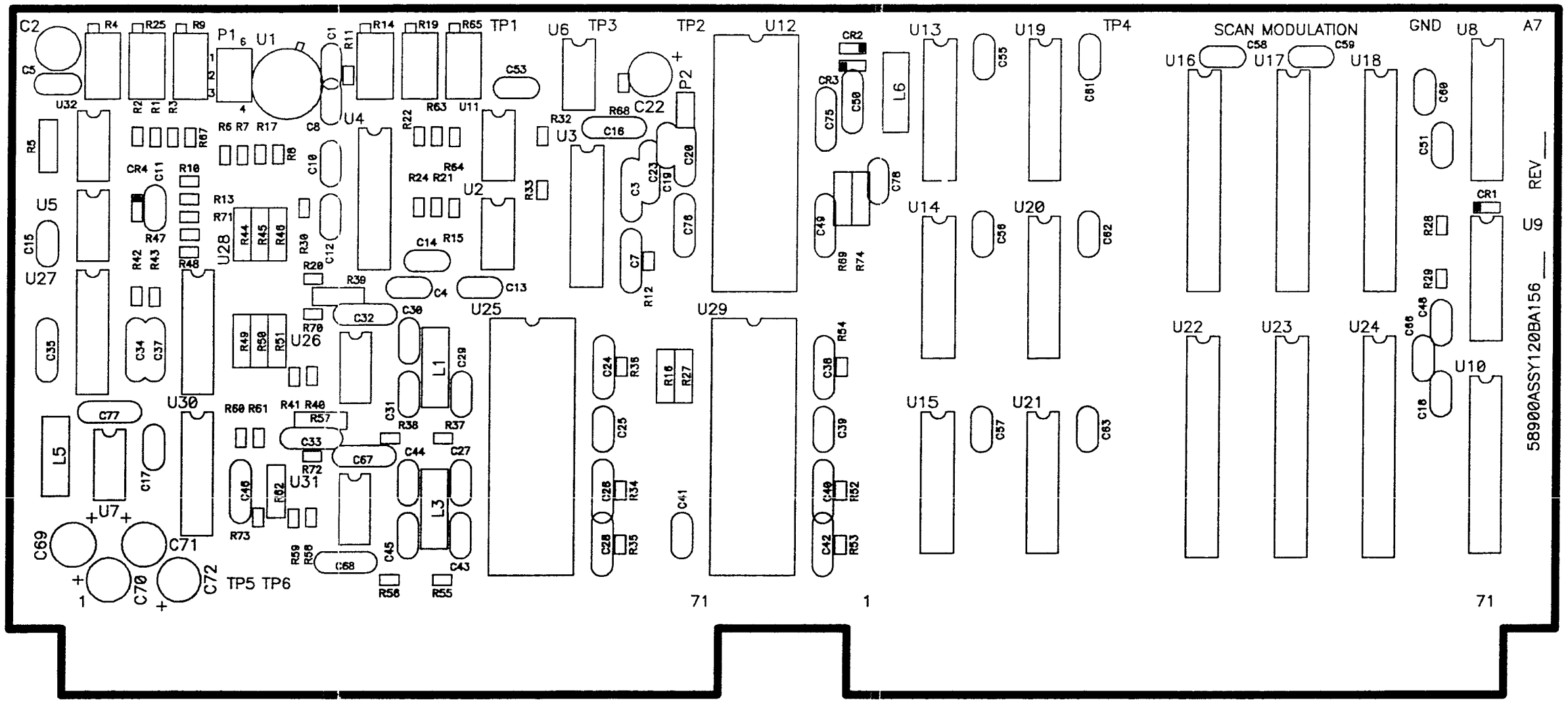
1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/4W, 1%
4. + INDICATES 1/5W, 1% RESISTORS



Function Generator (A6A1)
DWG# 120BM12601 Rev B
Sheet 4 of 4
7-A6-8



Scan Modulation (A7)
DWG# 120BM15600 Rev A
Sheet 1 of 5
7-A7-1



SCAN MODULATION -- PC ASSY A7

(Sheet 1) U10 decodes certain control inputs from the CPU; its outputs are used to activate the relay drivers (U7) for the scan module transfer switch, and also to activate the 17 MHz clock (U9) which drives the analog/digital conversion circuits.

The modulation inputs to this board are applied to U3-B, which switches between internally and externally generated modulation waveforms. There are two paths between U3-B and the second switch, U3-A, which switches between Scan and Fast AM modes. The AM path includes a logarithmic amplifier (U32-B, U1, U4, and U2-A) that is bypassed by the Scan path.

The output of U3A is supplied, by way of a DC amplifier (U5), to the analog-to-digital converter, U12. The ADC outputs are used to drive the address lines of volatile memories, shown on the sheet 2 of the diagram.

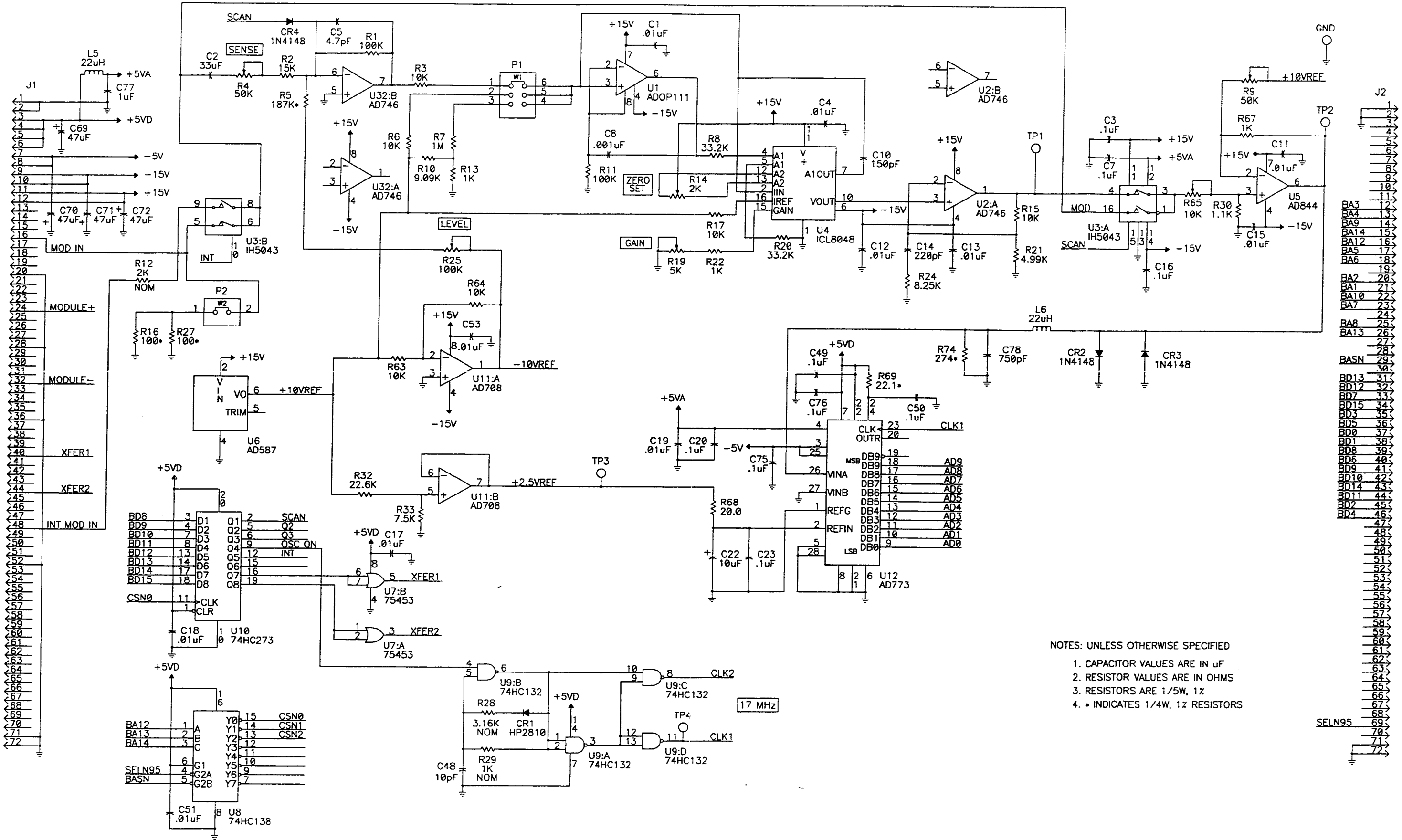
(Sheet 2) RAMs U16-U18 make up a 12-bit RAM which holds correction data for the scan module positive ('coarse') input. U22-U24 make up a 12-bit RAM which holds data for the negative ('fine') input. Both are applied to digital-to-analog converters shown on sheet 3 of the diagram.

Decoders U13-U15 control the address lines of RAMs U16-U18. The inputs to these address lines normally come from the ADC output (see sheet 1). However, when scan calibration points are reached, the inputs to the address lines come from the CPU, which uses the address lines to write new correction data into the RAMs. Input Q2 programs the decoders (U13-15) to connect either the CPU or the ADC to the address lines. The second set of decoders (U19-U21) serve the same function for the second set of RAMs (U22-U24).

(Sheet 3) The digital-to-analog converters (U25 and U29) convert the correction data from RAM into an analog value with which to drive the inputs of the scan modulator.

The output of DAC U25 is sent through a low-pass filter (see L1) to a high-current output amplifier consisting of U26, U27 and U28. This output provides the positive ('coarse') input to the scan modulator.

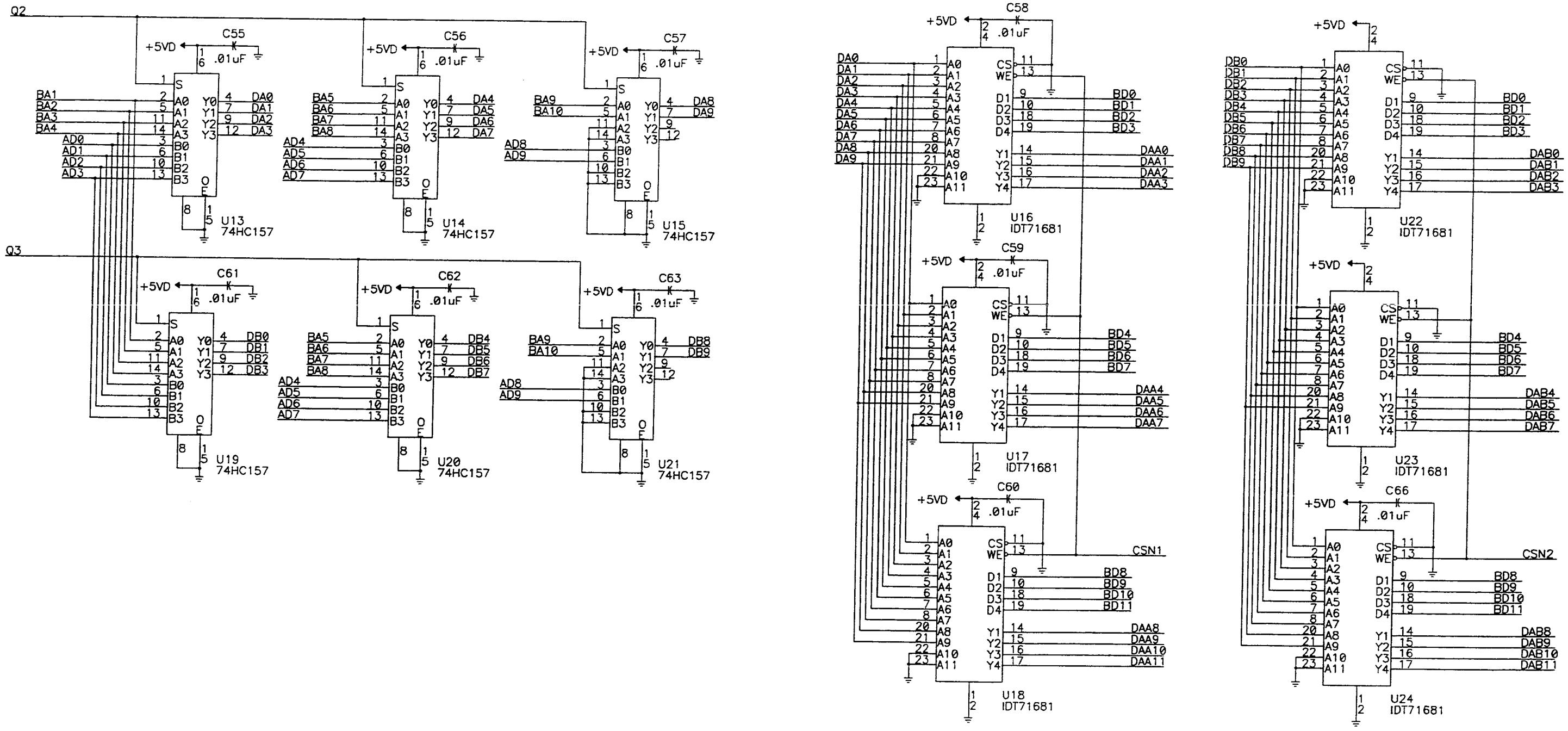
The output of DAC U29 is sent through a low pass filter (see L3) to a high-current output amplifier consisting of U31 and U30. This output provides the negative ('fine') input to the scan modulator.



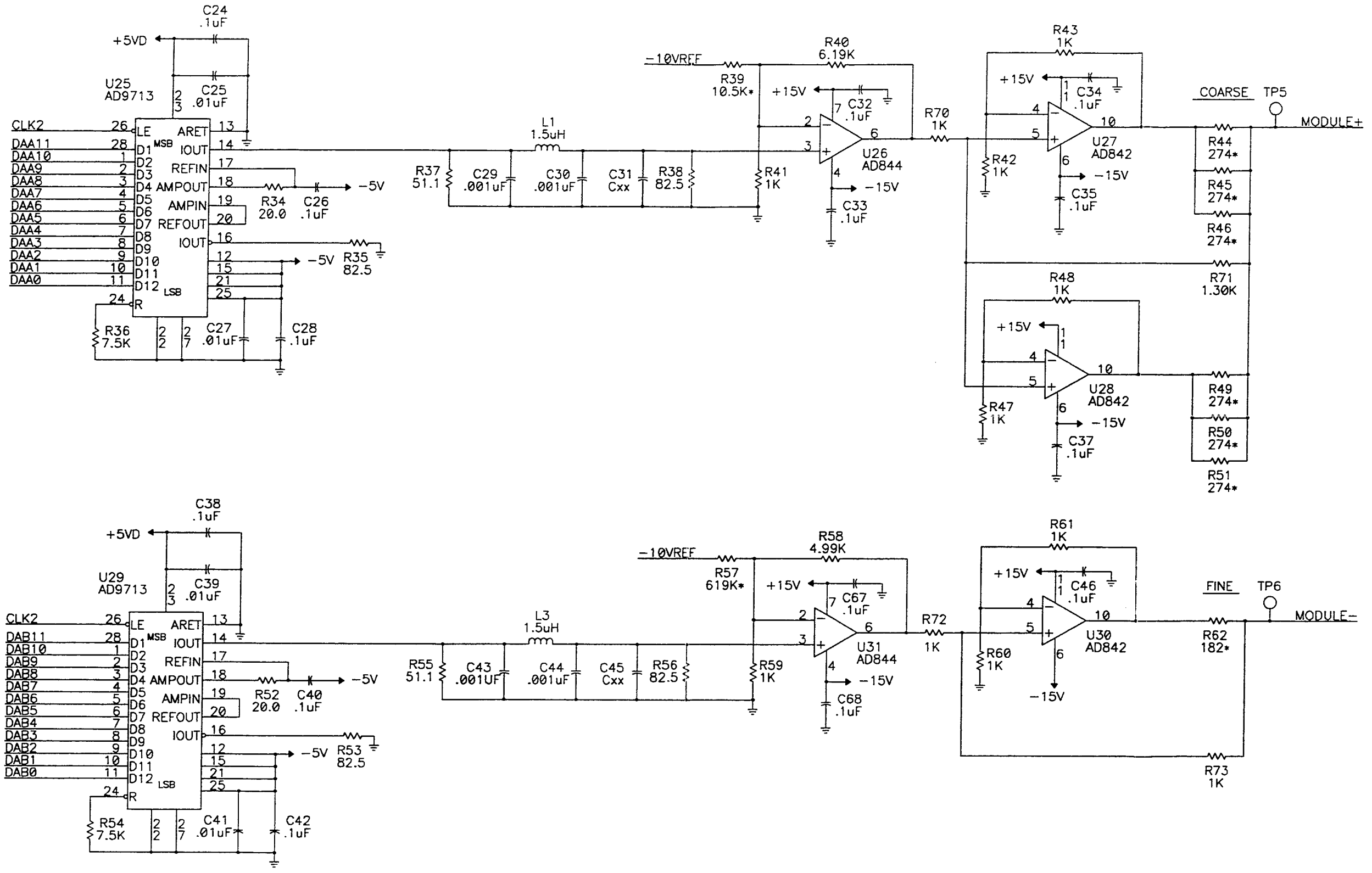
NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/5W, 1%
4. * INDICATES 1/4W, 1% RESISTORS

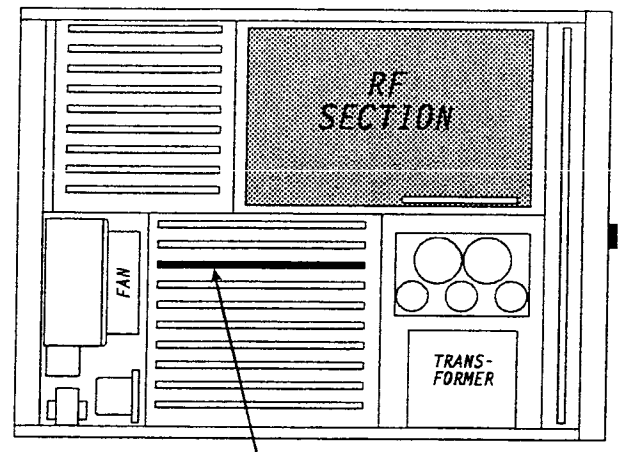
Scan Modulation (A7)
DWG# 120BM15600 Rev A
Sheet 3 of 5
7-A7-3



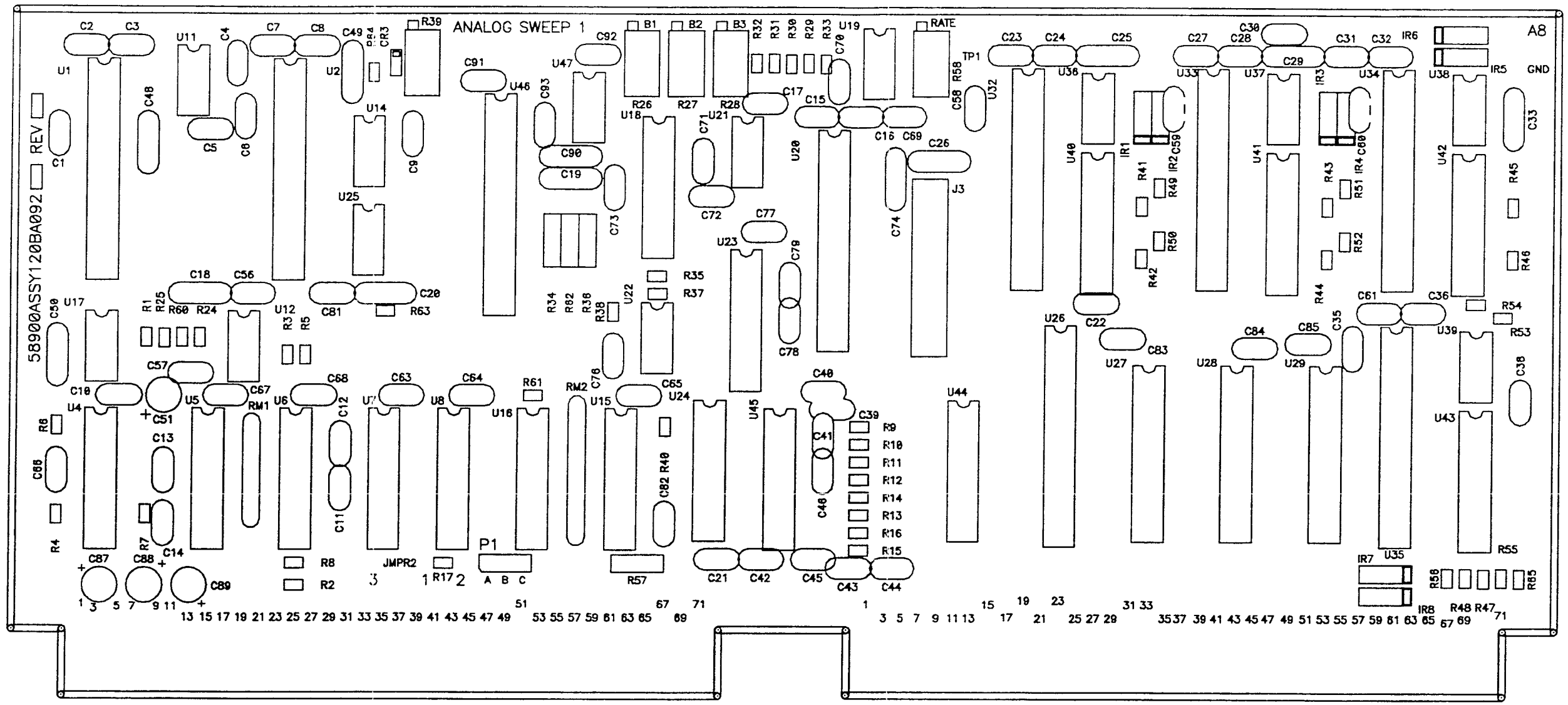
Scan Modulation (A7)
DWG# 120BM15600 Rev A
Sheet 4 of 5
7-A7-4



Scan Modulation (A7)
DWG# 120BM15600 Rev A
Sheet 5 of 5
7-A7-5



A8, A8A1



ANALOG SWEEP #1 – PC ASSY A8

The analog sweep board provides many signals required during analog sweep. The board has DACs which provide ramps for driving the main tune coils of the YIGs. It also has DACs to provide ramp voltages which trigger a number of comparators, thus generating various logic signals necessary to switch various filters and bands. Another set of DACs are used to control comparator reference voltages according to the marker frequencies which may be set. These comparators then generate the marker pulses.

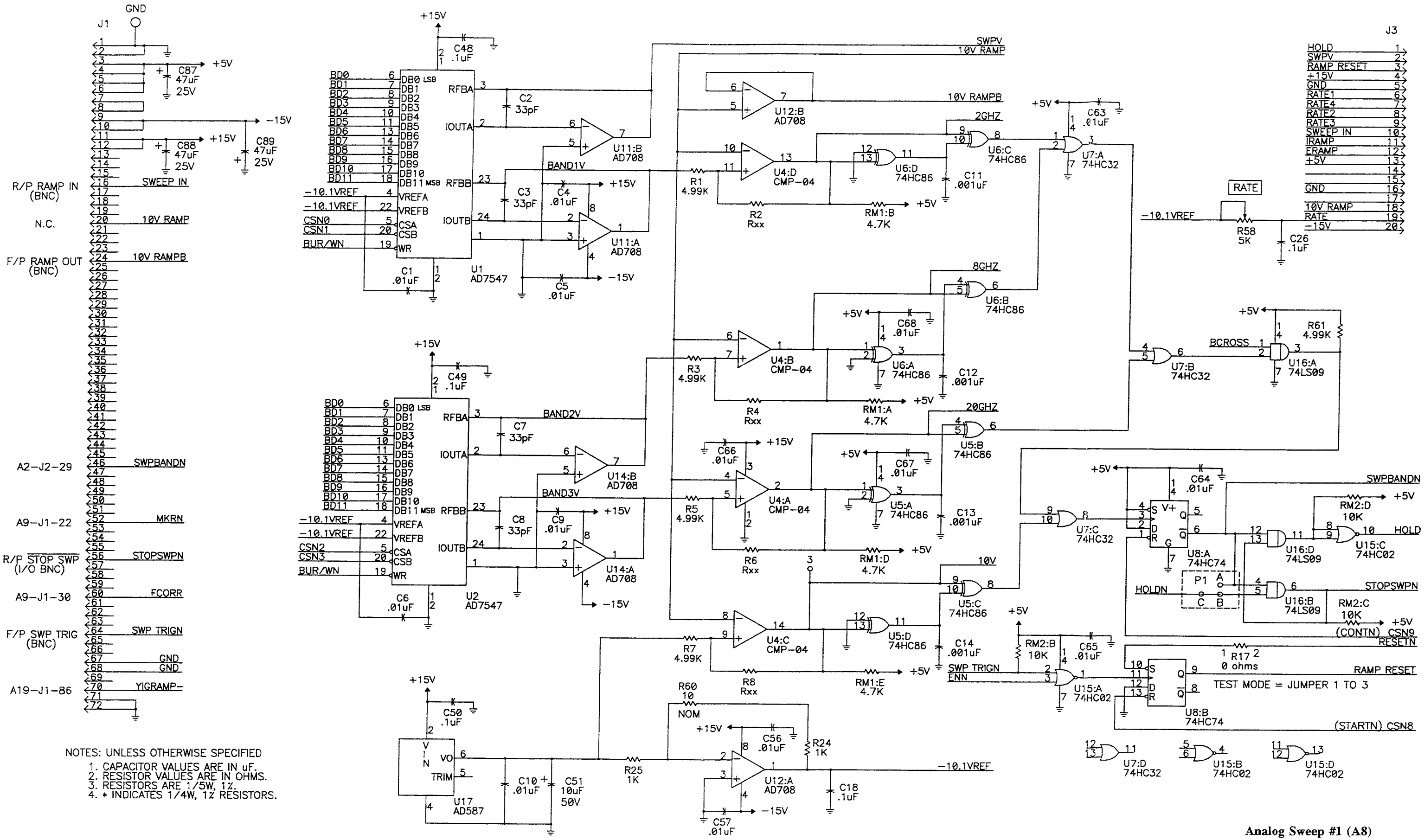
The DAC U1 section A gives a DC voltage at the output of U11 B which determines the rate at which the unit sweeps. DACs U1 B, U2 A and B are set up to give a voltage at the output of their respective amp (U11 A, U14 B and A) which corresponds to frequency band changes (at 2, 8 and 20 GHz). Specifically, for the 2 GHz band switch point the voltage from U11-1 is the reference voltage for comparator U4 D. The 10V_RAMP from A8A1 is the other input to the comparator. When the ramp voltage reaches the reference voltage the comparator switches, resulting in a pulse at U6-8 which propagates thru U7 and U16, clocking flip flop U8 A. This causes the Q-not output to go low signaling the computer that a band change must take place. This Q-not output also causes the hold line (U15-10) to trigger thereby stopping the ramp on the A8A1 board. In addition the signal is output to the rear panel as the STOP SWP I/O logic signal. When the band change is complete the computer sends a signal CONTN to reset the flip flop U8. The 8 and 20 GHz band changes work similarly.

The 10 volt reference from U17 is inverted by U12 giving a negative reference. The +10V reference is used as the reference for the U4 C comparator. This comparator switches at the end of each sweep and generates a pulse. When the SWP_TRIGN signal is received, (this signal is produced by the front panel SWP TRIG input) U15 A and U8 B cause the RAMP_RESET line to reset the ramp voltage on A8A1.

The 10V_RAMP is applied to U19 A where it is inverted and then summed at U19 B with different offset voltages, switched by U18, at each band change. These offset voltages cause the ramp at U19-7 to start at 0V for each new band. The amplitude of the ramps are then adjusted by DAC U20 section A and B (using both sections gives a greater range). The resulting ramp is buffered by U47 B and summed together at U22 B with other signals, including the frequency correction signal from the digital ramp board A9. The switch U23 can then select the ramp or an inverted version of this ramp (U22 A) for output to the YIG driver, depending on whether the frequency sweep is increasing or decreasing. Another signal is summed into the ramp at U22 B; this signal is YIG lag compensation. At the start of each band U16 C triggers U24 A causing a pulse at the Q not output. The negative going pulse at U25 A is turned into a negative going spike with decay by the diode CR3 and C20. This is buffered by U25 B and its amplitude is adjusted by DAC U46 according to the sweep rate. The amplitude of the spike is maximum for the highest sweep rate. The output of U47 A is then summed with the frequency correction and the ramp voltage at U22 B.

U32 thru U35 DACs provide reference voltages for up to 8 analog sweep markers. For example, when a marker is set, DAC U32 A generates a reference voltage at U36-7 for comparators U40 C and D. When the 10V_RAMP reaches the reference voltage the comparators flip, generating a marker pulse at the output U40 pin 13 and 14. The width of this pulse is determined by IR1 and R41. The pulse then propagates thru U45 and is buffered to be supplied to the rear panel. The rest of the markers are generated in the same way and are NOR'ed together at U45.

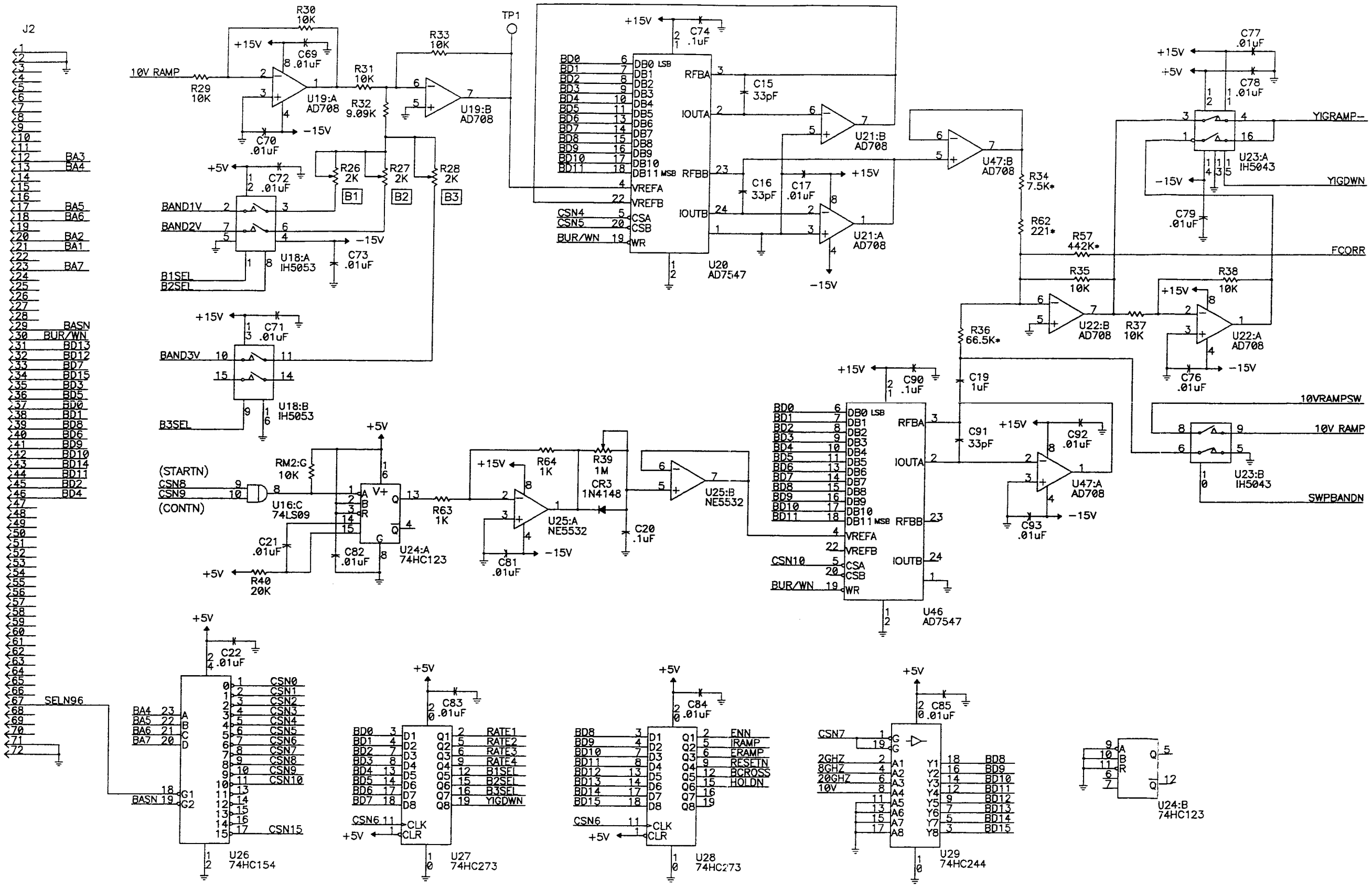
U44 and U26 decode chip selects for the board. U27, U28 and U29 provide buffering necessary for computer bus interface.



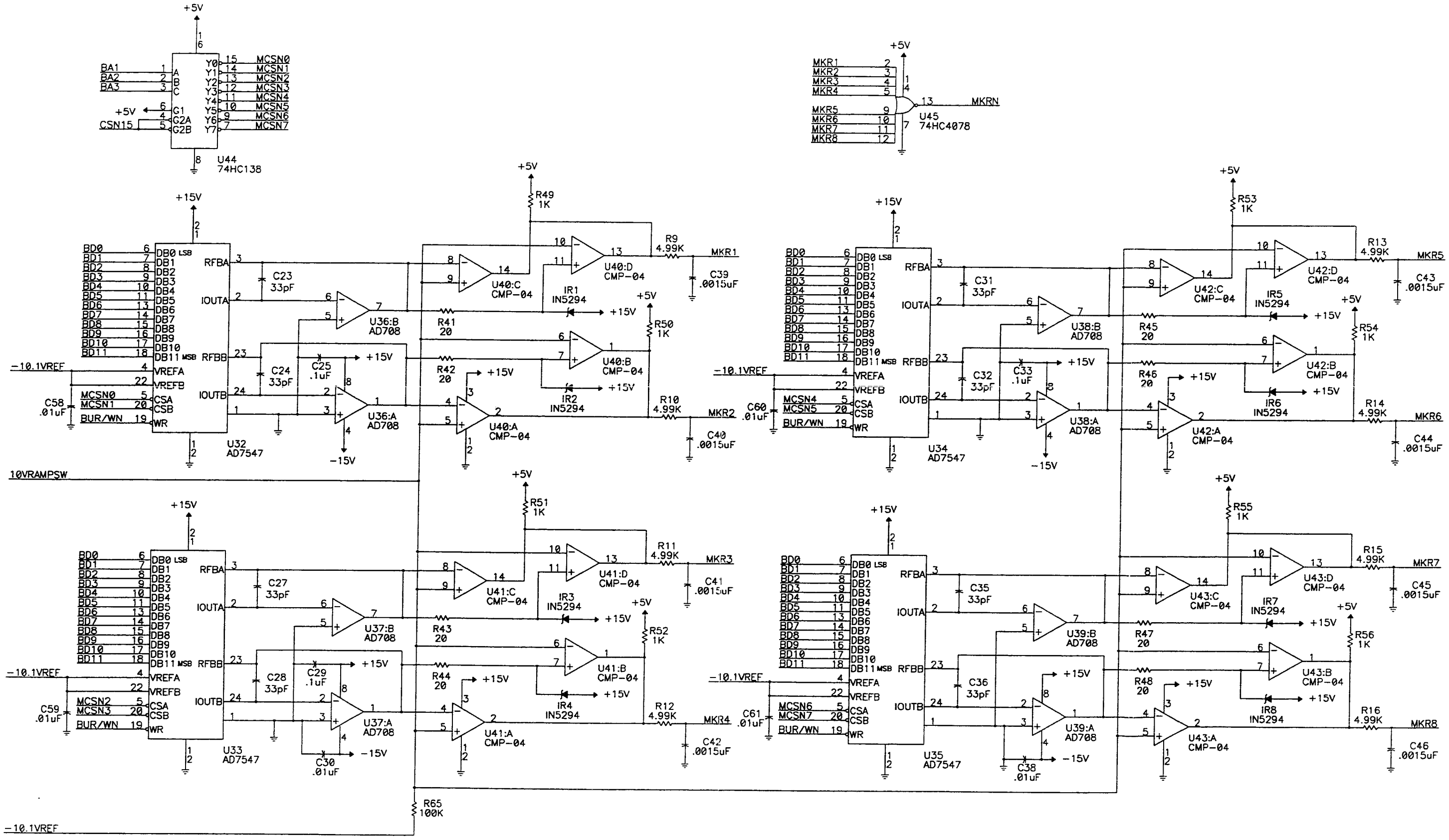
NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN uF.
2. RESISTOR VALUES ARE IN OHMS.
3. RESISTORS ARE 1/5W, 1%.
4. * INDICATES 1/4W, 1% RESISTORS.

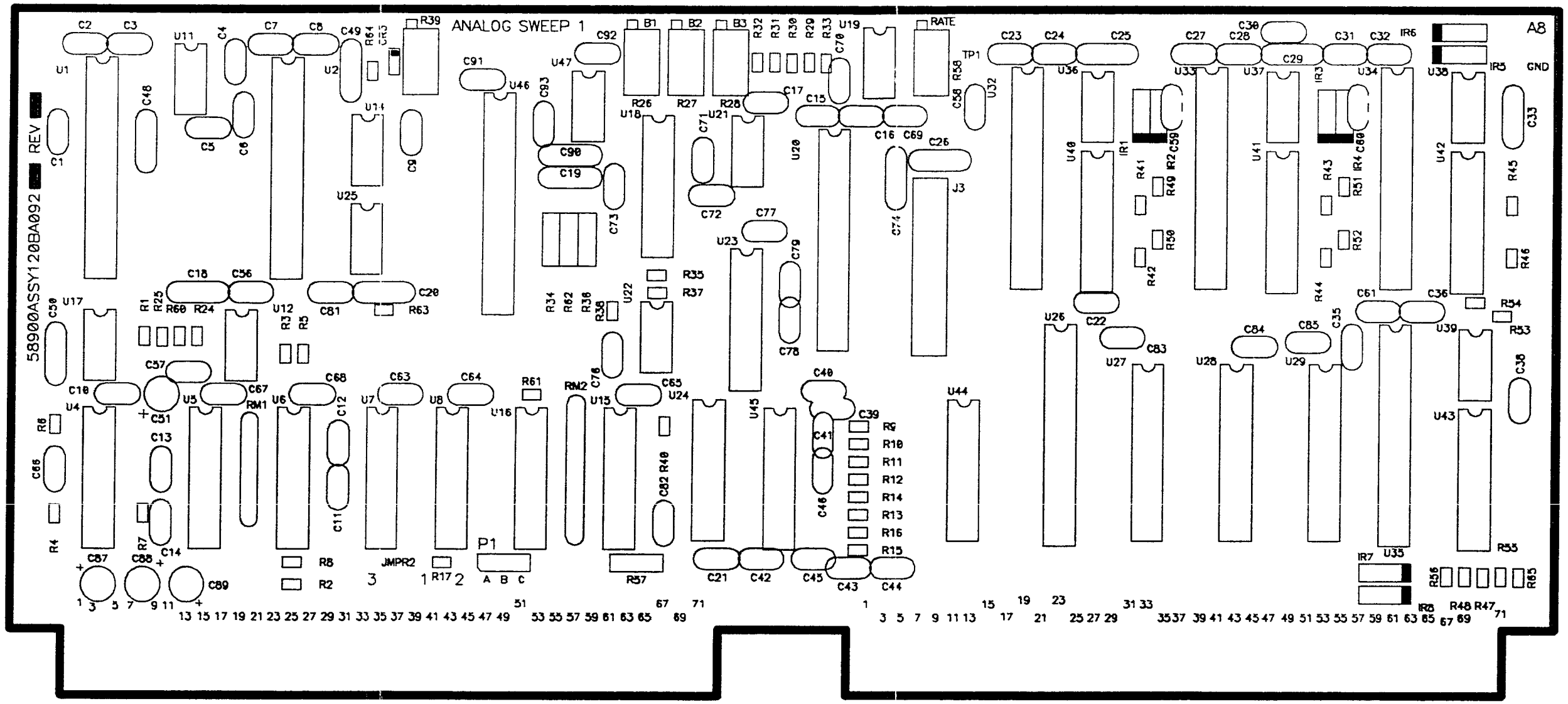
Analog Sweep #1 (A8)
DWG# 120BM09211 Rev A
Sheet 3 of 5
7-A8-3



Analog Sweep #1 (A8)
DWG# 120BM09211 Rev A
Sheet 4 of 5
7-A8-4



Analog Sweep #1 (A8)
DWG# 120BM09211 Rev A
Sheet 5 of 5
7-A8-5



ANALOG SWEEP #1 -- PC ASSY A8

The analog sweep board provides many signals required during analog sweep. The board has DACs which provide ramps for driving the main tune coils of the YIGs. It also has DACs to provide ramp voltages which trigger a number of comparators, thus generating various logic signals necessary to switch various filters and bands. Another set of DACs are used to control comparator reference voltages according to the marker frequencies which may be set. These comparators then generate the marker pulses.

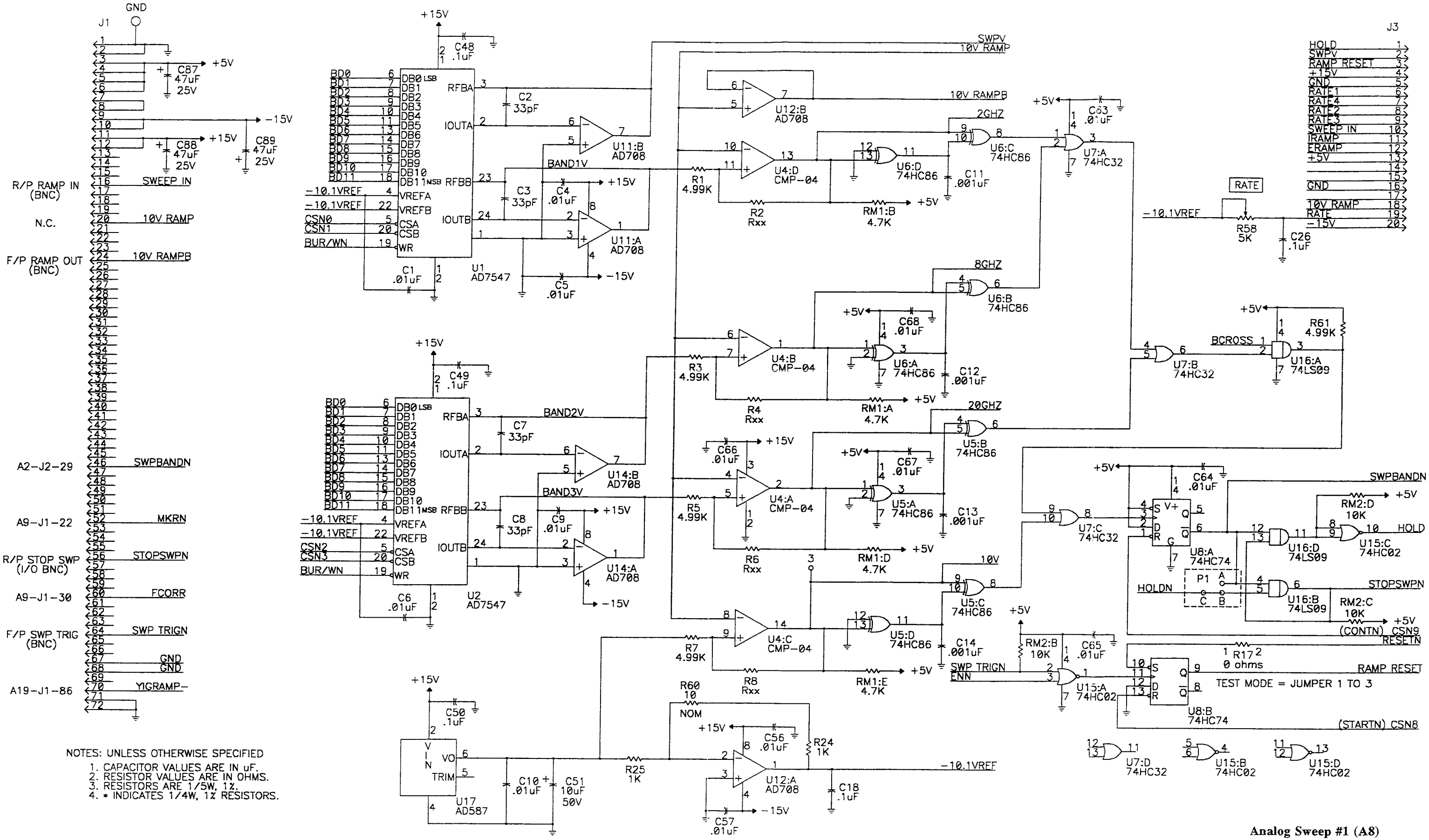
The DAC U1 section A gives a DC voltage at the output of U11 B which determines the rate at which the unit sweeps. DACs U1 B, U2 A and B are set up to give a voltage at the output of their respective amp (U11 A, U14 B and A) which corresponds to frequency band changes (at 2, 8 and 20 GHz). Specifically, for the 2 GHz band switch point the voltage from U11-1 is the reference voltage for comparator U4 D. The 10V_RAMP from A8A1 is the other input to the comparator. When the ramp voltage reaches the reference voltage the comparator switches, resulting in a pulse at U6-8 which propagates thru U7 and U16, clocking flip flop U8 A. This causes the Q-not output to go low signaling the computer that a band change must take place. This Q-not output also causes the hold line (U15-10) to trigger thereby stopping the ramp on the A8A1 board. In addition the signal is output to the rear panel as the STOP SWP I/O logic signal. When the band change is complete the computer sends a signal CONTN to reset the flip flop U8. The 8 and 20 GHz band changes work similarly.

The 10 volt reference from U17 is inverted by U12 giving a negative reference. The +10V reference is used as the reference for the U4 C comparator. This comparator switches at the end of each sweep and generates a pulse. When the SWP_TRIGN signal is received, (this signal is produced by the front panel SWP TRIG input) U15 A and U8 B cause the RAMP_RESET line to reset the ramp voltage on A8A1.

The 10V_RAMP is applied to U19 A where it is inverted and then summed at U19 B with different offset voltages, switched by U18, at each band change. These offset voltages cause the ramp at U19-7 to start at 0V for each new band. The amplitude of the ramps are then adjusted by DAC U20 section A and B (using both sections gives a greater range). The resulting ramp is buffered by U47 B and summed together at U22 B with other signals, including the frequency correction signal from the digital ramp board A9. The switch U23A can then select the ramp or an inverted version of this ramp (U22 A) for output to the YIG driver, depending on whether the frequency sweep is increasing or decreasing. Another signal is summed into the ramp at U22 B; this signal is YIG lag compensation. At the start of each band U16 C triggers U24 A causing a pulse at the Q not output. The negative going pulse at U25 A is turned into a negative going spike with decay by the diode CR3 and C20. This is buffered by U25 B and its amplitude is adjusted by DAC U46 according to the sweep rate. The amplitude of the spike is maximum for the highest sweep rate. The output of U47 A is then summed with the frequency correction and the ramp voltage at U22 B.

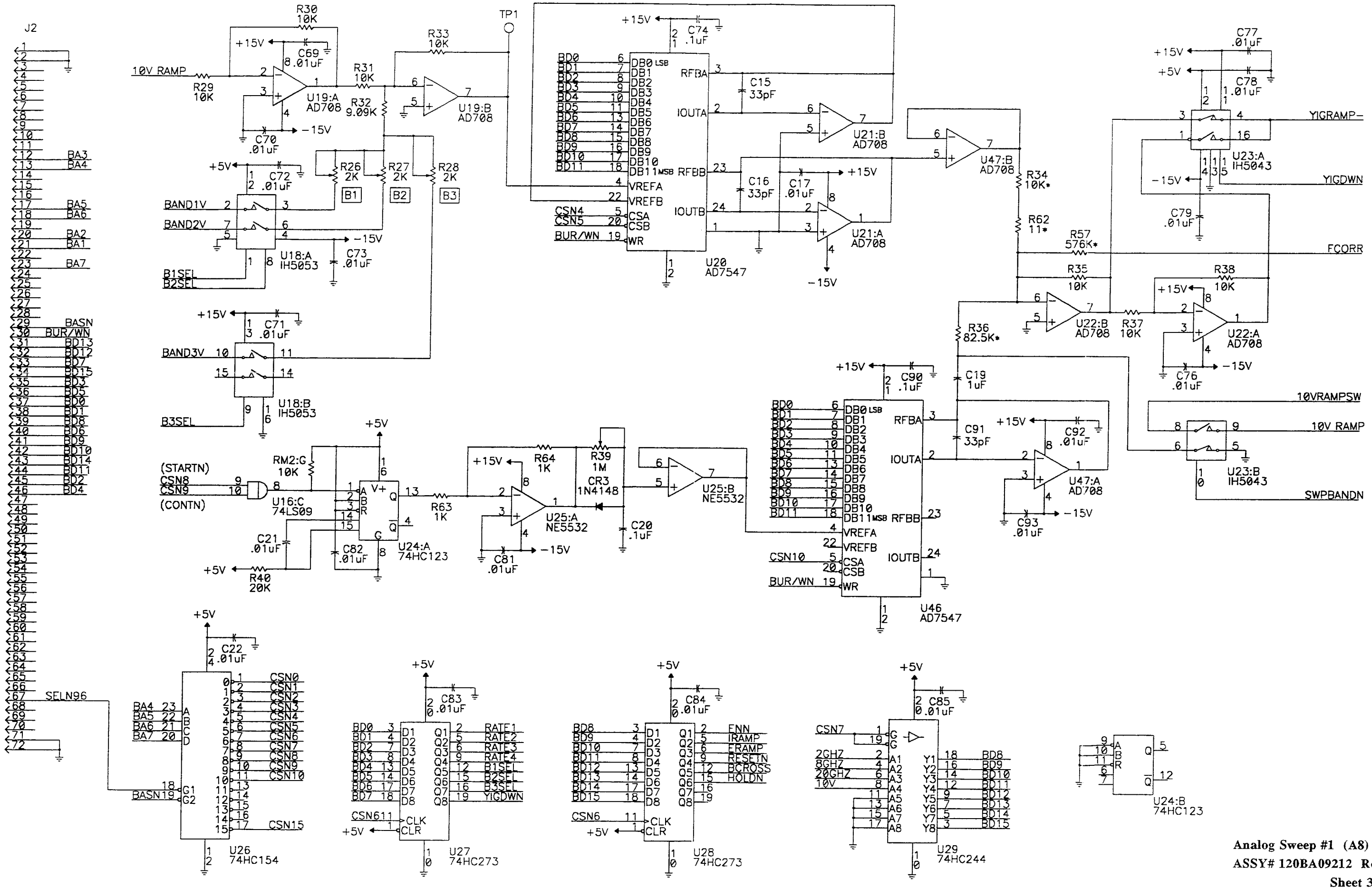
U32 thru U35 DACs provide reference voltages for up to 8 analog sweep markers. For example, when a marker is set, DAC U32 A generates a reference voltage at U36-7 for comparators U40 C and D. When the 10V_RAMP reaches the reference voltage the comparators flip, generating a marker pulse at the output U40 pin 13 and 14. The width of this pulse is determined by IR1 and R41. The pulse then propagates thru U45 and is buffered to be supplied to the rear panel. The rest of the markers are generated in the same way and are NOR'ed together at U45.

U44 and U26 decode chip selects for the board. U27, U28 and U29 provide buffering necessary for computer bus interface.

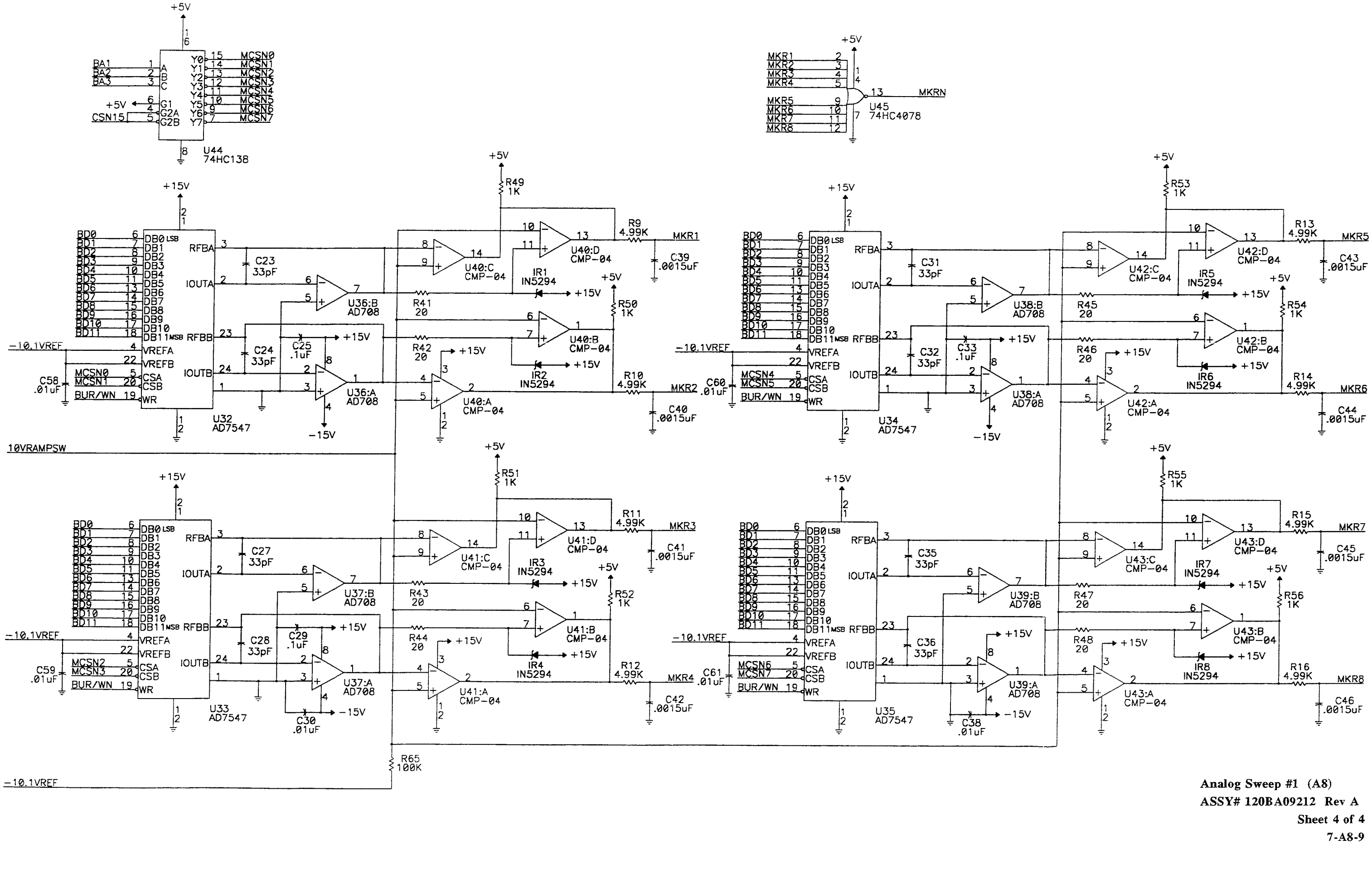


NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITOR VALUES ARE IN uF.
2. RESISTOR VALUES ARE IN OHMS.
3. RESISTORS ARE 1/5W, 1%.
4. * INDICATES 1/4W, 1% RESISTORS.

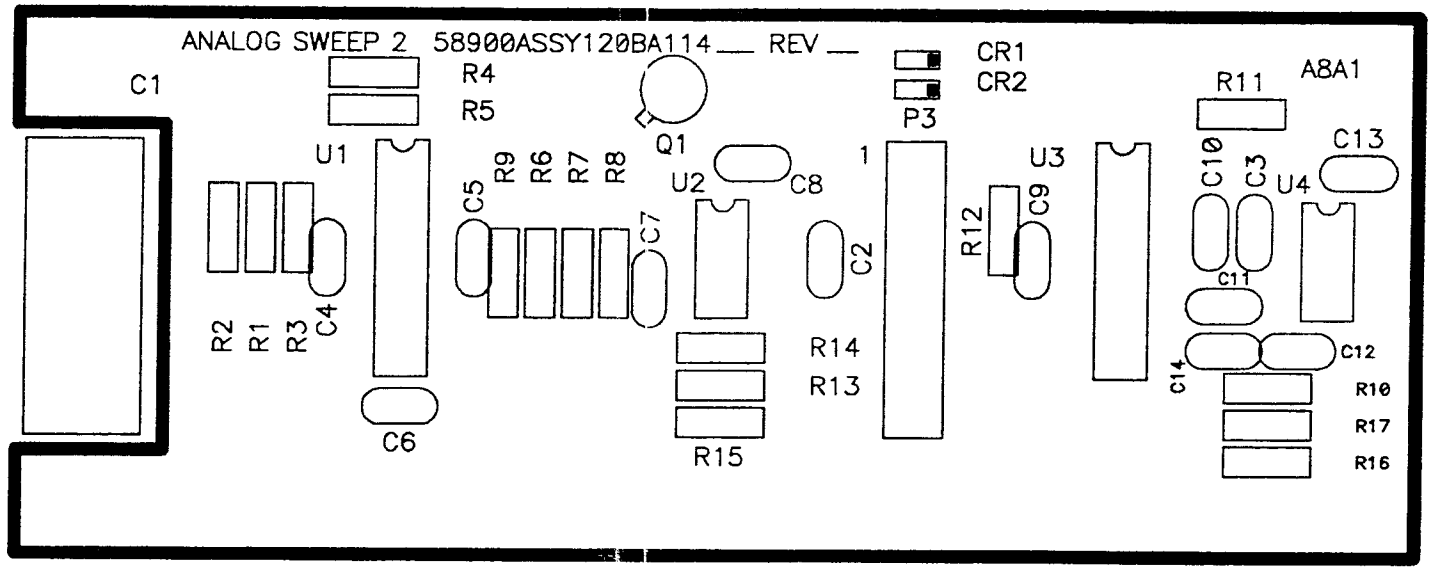
Analog Sweep #1 (A8)
ASSY# 120BA09212 Rev A
Sheet 2 of 4
7-A8-7



Analog Sweep #1 (A8)
ASSY# 120BA09212 Rev A
Sheet 3 of 4
7-A8-8



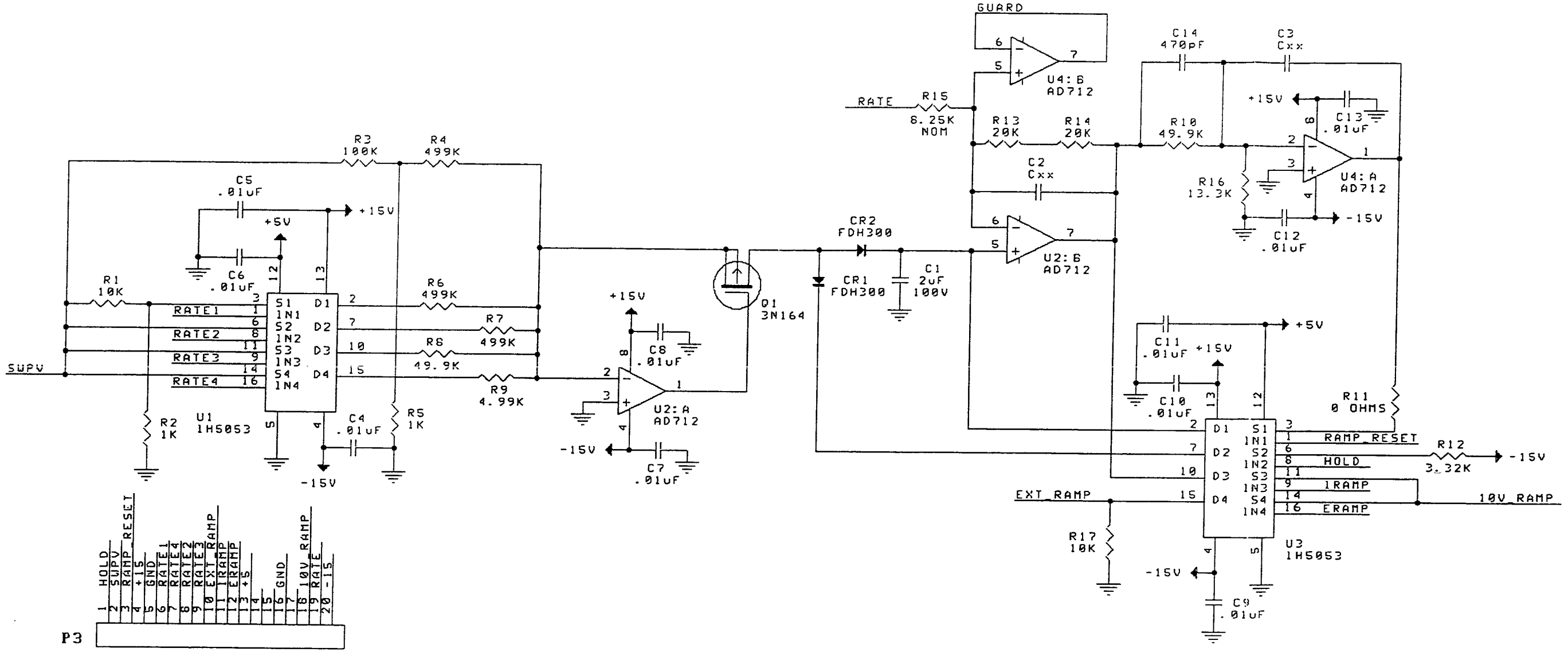
Analog Sweep #1 (A8)
ASSY# 120BA09212 Rev A
Sheet 4 of 4
7-A8-9



ANALOG SWEEP #2 -- PC ASSY A8A1

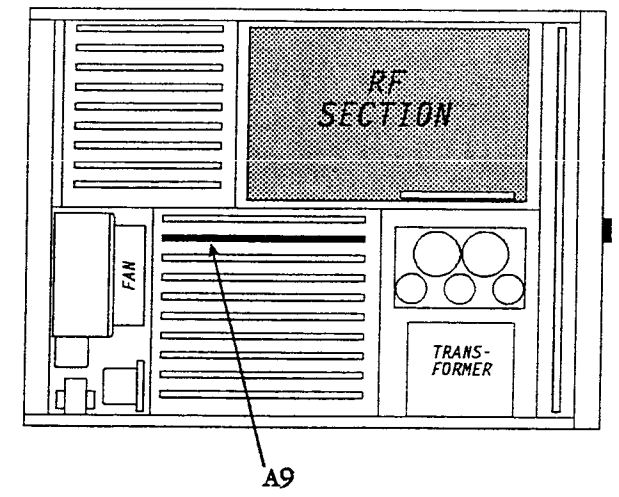
The main function of this board is to generate the various sweep rates.

A DC voltage SWPV is received from the A8 board whose magnitude varies according to the sweep rate selected. U1 switches resistors in parallel with R3 and R4 which gives decade changes in the rate by switching the current flow generated by the current source U2 A and Q1. The rates are controlled by the rate at which the cap C1 charges. The charging cap results in a ramp at U2-7 which can be fine tuned by the rate voltage summed into U2 B. This 0-10V ramp or an external ramp can be selected by U3 as the 10V ramp output. U4 A is used for the purpose of resetting the rate ramp, when RAMP_RESET is selected at U3, by pulling U2-7 to 0V. When HOLD is selected CR1 cathode is pulled low, sinking current from the current source and biasing CR2 such that the voltage on C1 is held constant. This allows the ramp voltage to be held during band crossovers.

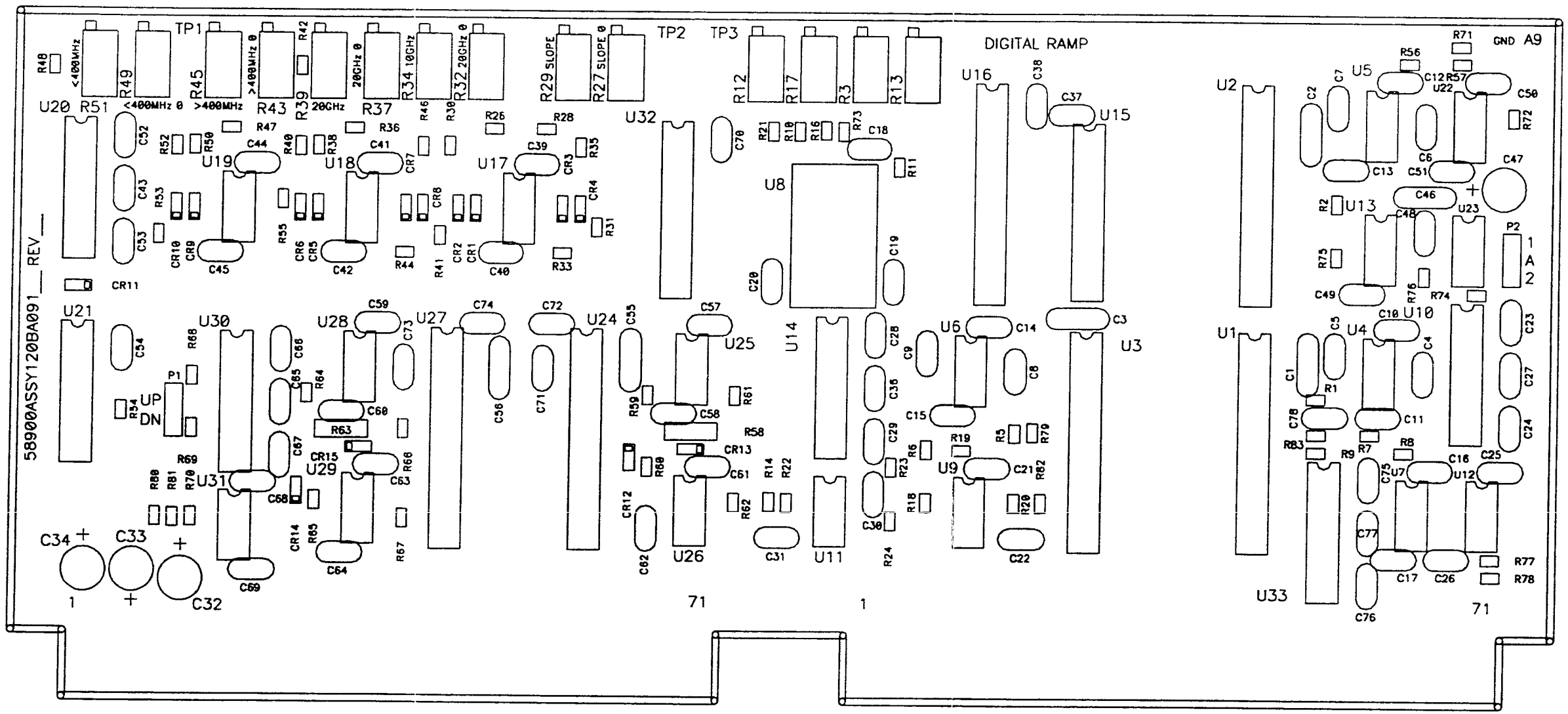


NOTES: UNLESS OTHERWISE SPECIFIED

1) CAPACITOR VALUES ARE IN uF
2) RESISTOR VALUES ARE IN OHMS
3) RESISTORS ARE 1/4W, 1%



Digital Ramp (A9)
DWG# 120BM09100 Rev F
Sheet 1 of 4
7-A9-1



DIGITAL RAMP PCA -- PC ASSY A9

The Digital Ramp PCA circuitry includes circuitry which generates voltage ramps required for both analog and digital sweep modes. It also provides level correction and frequency correction data required during analog sweep.

The DAC U1 section generates a 0 to 10V digital frequency ramp available at the output of U4 B. U10 B is used to switch either this digital frequency ramp or a 10 Volt ramp from the analog sweep board which is supplied to U12 B which provides the ramp output voltage to the front panel. The output of U10 B switch is also provided to U22 B which inverts the ramp. The frequency ramp or the negative frequency ramp is selected by U33 B depending on the direction of the sweep. The ramp selected is the input to the B section of DAC U1 which multiplies the ramp by some factor resulting in a ramp output at U4 A which is proportional to the delta or width of the sweep. DAC U2 section A provides a DC output voltage at U5 B which is proportional to the start frequency of the sweep. This start frequency voltage and the voltage ramp are summed together at U7 A resulting in a -.5 Volt per GHz ramp. This signal and an inverted form of the same signal (U7-7) are used by the level correction circuitry. The .5 V/GHz signal is also buffered by U12 A for output to the Rear Panel.

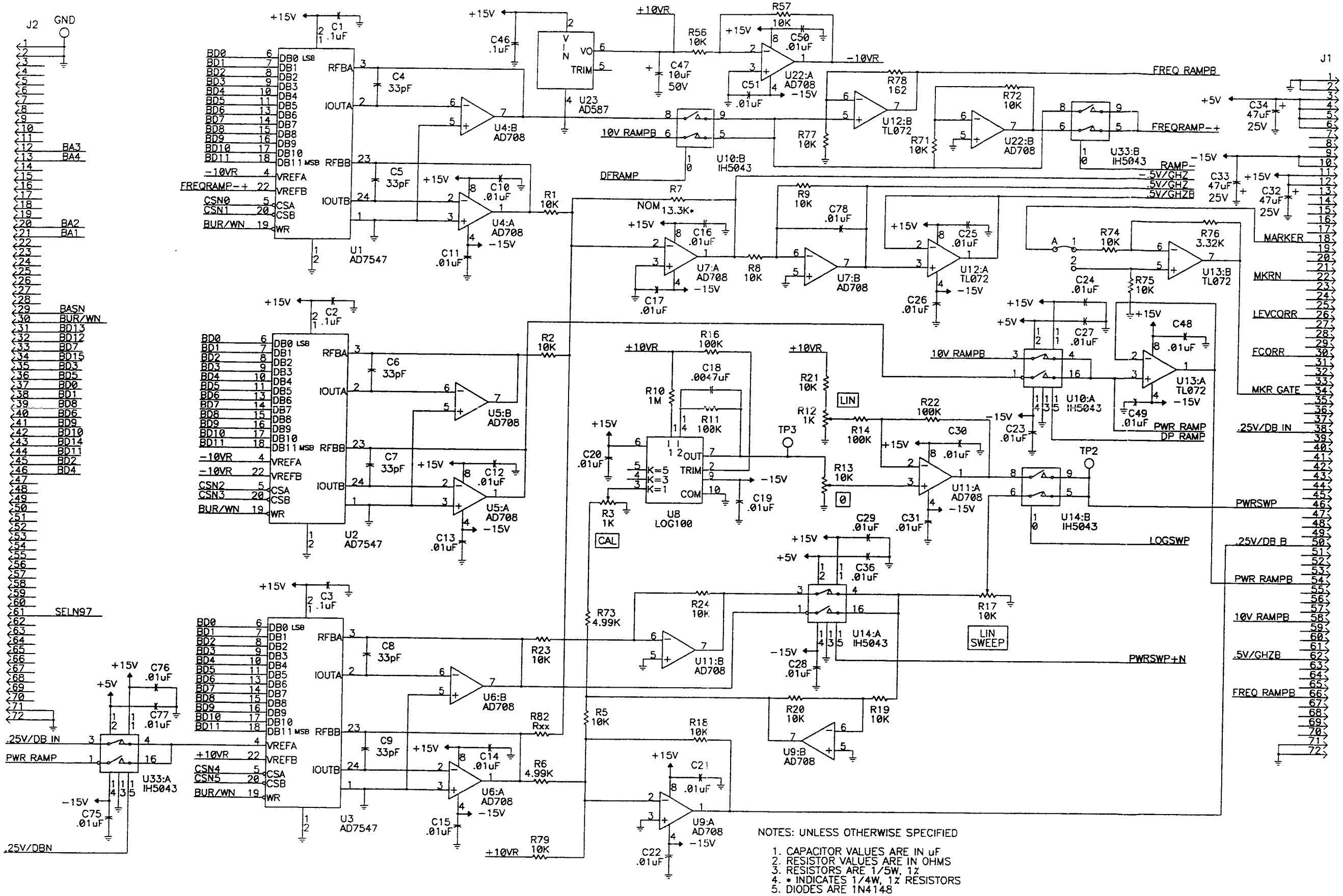
Section B of U2 generates a 0 to 10 Volt digital power ramp available at U5-1. This ramp or a 10 Volt ramp from the analog sweep board is selected by U10 A to be buffered by U13 A for optional Power Ramp to the rear panel, and to be fed back to U33 A. U33 A is used to switch the power ramp or a .5V/DB input (optional) from the rear panel, to the input of DAC U3 section A which multiplies the ramp by some factor resulting in a ramp output at U6-7 which is proportional to the delta or width of the power sweep. This delta power ramp or its inverse (U11 B) is selected by switch U14 A. It is inverted again at U9 B and summed at U9 A with a voltage proportional to the start power. This voltage is generated by DAC U3 and U6 A, resulting in a signal out at U9-1 which is .1V/ DB an optional rear panel output. The delta power ramp amplitude can also be calibrated by R3 before it is anti-logged by U8. U8 output is shifted and offset appropriately (R13 and R12) so that at the output of U11 A the delta power ramp is linear in dB. Either this signal or the straight delta power ramp (calibrated at R17) is selected at U14 B providing a power sweep voltage, linear in voltage or in dB, to the level control board.

The level correction circuitry requires the +.5V/GHz and - .5V/GHz ramp inputs as well as a + and - 10V reference. U17 B and U18 A along with their corresponding pots allow the ramp signal to be modified by 2 different slopes. The pots R32 and R37 allow the different slopes (controlled by R34 and R39) to start at different places corresponding to different frequencies. The resulting modified ramp is selected by U20 A to be used for frequencies greater than 2 GHz. There are two slope adjustments, U18 B and U19 A and corresponding pots, which can be selected to be used at frequencies less than 2GHz. To these slopes, specific to > or < 2GHz frequency bands, is added an additional universal slope, created by U17 A and its pots R27 and R29. This addition takes place at U19 B where yet another input may be selected by U20 B. This input is the amplitude marker input, which when enabled, pulses the instrument's output level at a frequency set by the marker. The final level correction voltage is available at U19-7 and is summed into the level board A10.

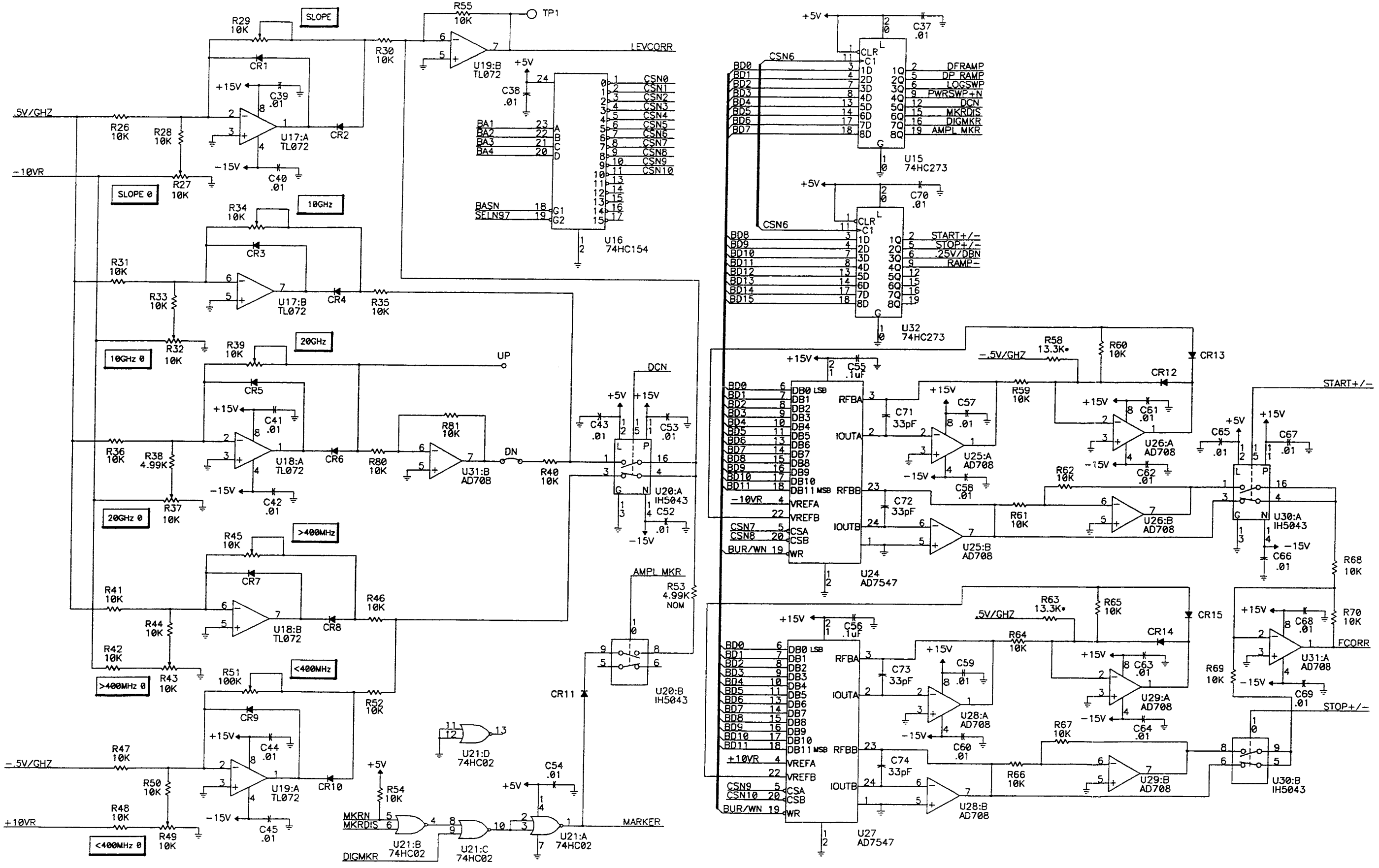
U13 B input is the marker signal which is amplified by U13 B to provide an optional rear panel output MKR_GATE which is provided for the purpose of gating an external counter.

U23 provides a +10 volt reference which is also inverted by U22 A giving a -10 volt reference as well. U32 and U15 provide the necessary buffering for interfacing with the computer bus. U16 decodes chip select lines.

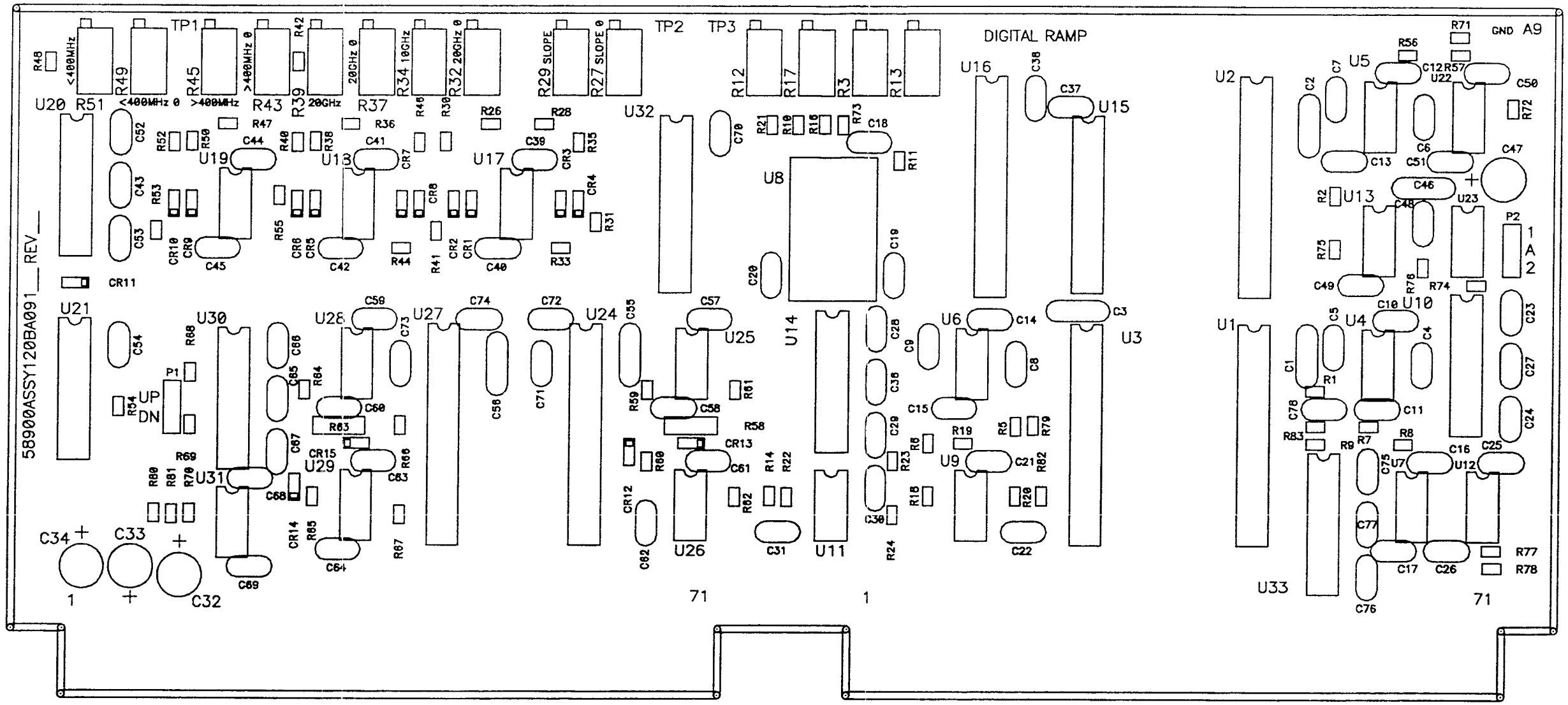
U24 and U27 digitally generate a similar slope correction as is created by the level correction circuitry. U24 DAC section A provides a DC offset voltage at U25-1 which controls what frequency (or voltage) the slope (in this case generated by -.5V/GHz ramp) summed into U26 A, begins having an effect. The steepness of this slope is then adjusted by the DAC when the signal is fed back into section B. The result is an output at U25-7 which has some specific slope starting at some specific frequency. This slope or its inverse is selected (U30 A) and summed together with another similar slope signal (generated by U27, U28 and U29). The result is a frequency correction signal at U31-1, which is summed with the YIG ramp on the A8 board, to keep the frequency correct during analog sweep.



Digital Ramp (A9)
DWG# 120BM09100 Rev F
Sheet 3 of 4
7-A9-3



Digital Ramp (A9)
DWG# 120BM09100 Rev F
Sheet 4 of 4
7-A9-4



DIGITAL RAMP PCA -- PC ASSY A9

The Digital Ramp PCA circuitry includes circuitry which generates voltage ramps required for both analog and digital sweep modes. It also provides level correction and frequency correction data required during analog sweep.

The DAC U1 section generates a 0 to 10V digital frequency ramp available at the output of U4 B. U10 B is used to switch either this digital frequency ramp or a 10 Volt ramp from the analog sweep board which is supplied to U12 B which provides the ramp output voltage to the front panel. The output of U10 B switch is also provided to U22 B which inverts the ramp. The frequency ramp or the negative frequency ramp is selected by U33 B depending on the direction of the sweep. The ramp selected is the input to the B section of DAC U1 which multiplies the ramp by some factor resulting in a ramp output at U4 A which is proportional to the delta or width of the sweep. DAC U2 section A provides a DC output voltage at U5 B which is proportional to the start frequency of the sweep. This start frequency voltage and the voltage ramp are summed together at U7 A resulting in a -.5 Volt per GHz ramp. This signal and an inverted form of the same signal (U7-7) are used by the level correction circuitry. The .5 V/GHz signal is also buffered by U12 A for output to the Rear Panel.

Section B of U2 generates a 0 to 10 Volt digital power ramp available at U5-1. This ramp or a 10 Volt ramp from the analog sweep board is selected by U10 A to be buffered by U13 A for optional Power Ramp to the rear panel, and to be fed back to U33 A. U33 A is used to switch the power ramp or a .5V/DB input (optional) from the rear panel, to the input of DAC U3 section A which multiplies the ramp by some factor resulting in a ramp output at U6-7 which is proportional to the delta or width of the power sweep. This delta power ramp or its inverse (U11 B) is selected by switch U14 A. It is inverted again at U9 B and summed at U9 A with a voltage proportional to the start power. This voltage is generated by DAC U3 and U6 A, resulting in a signal out at U9-1 which is .1V/ DB an optional rear panel output. The delta power ramp amplitude can also be calibrated by R3 before it is anti-logged by U8. U8 output is shifted and offset appropriately (R13 and R12) so that at the output of U11 A the delta power ramp is linear in dB. Either this signal or the straight delta power ramp (calibrated at R17) is selected at U14 B providing a power sweep voltage, linear in voltage or in dB, to the level control board.

The level correction circuitry requires the +.5V/GHz and - .5V/GHz ramp inputs as well as a + and - 10V reference. U17 B and U18 A along with their corresponding pots allow the ramp signal to be modified by 2 different slopes. The pots R32 and R37 allow the different slopes (controlled by R34 and R39) to start at different places corresponding to different frequencies. The resulting modified ramp is selected by U20 A to be used for frequencies greater than 2 GHz. There are two slope adjustments, U18 B and U19 A and corresponding pots, which can be selected to be used at frequencies less than 2GHz. To these slopes, specific to > or < 2GHz frequency bands, is added an additional universal slope, created by U17 A and its pots R27 and R29. This addition takes place at U19 B where yet another input may be selected by U20 B. This input is the amplitude marker input, which when enabled, pulses the instrument's output level at a frequency set by the marker. The final level correction voltage is available at U19-7 and is summed into the level board A10.

U13 B input is the marker signal which is amplified by U13 B to provide an optional rear panel output MKR_GATE which is provided for the purpose of gating an external counter.

U23 provides a +10 volt reference which is also inverted by U22 A giving a -10 volt reference as well. U32 and U15 provide the necessary buffering for interfacing with the computer bus. U16 decodes chip select lines.

U24 and U27 digitally generate a similar slope correction as is created by the level correction circuitry. U24 DAC section A provides a DC offset voltage at U25-1 which controls what frequency (or voltage) the slope (in this case generated by -.5V/GHz ramp) summed into U26 A, begins having an effect. The steepness of this slope is then adjusted by the DAC when the signal is fed back into section B. The result is an output at U25-7 which has some specific slope starting at some specific frequency. This slope or its inverse is selected (U30 A) and summed together with another similar slope signal (generated by U27, U28 and U29). The result is a frequency correction signal at U31-1, which is summed with the YIG ramp on the A8 board, to keep the frequency correct during analog sweep.

J2 GND
1 2 3 4 5 6 7 8 9 10 11 12 BA3 13 BA4 14 15 16 17 18 19 20 BA2 21 BA1 22 23 24 25 26 27 28 29 BASN 30 BUR/WN 31 BD13 32 BD12 33 BD7 34 BD15 35 BD3 36 BD5 37 BD0 38 BD1 39 BD8 40 BD6 41 BD9 42 BD10 43 BD14 44 BD11 45 BD2 46 BD4 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 SELN97 62 63 64 65 66 67 68 69 70 71 72

J1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 MARKER 19 20 21 22 MKRN 23 24 25 26 LEVCORR 27 28 29 30 FCORR 31 32 33 34 MKR GATE 35 36 37 38 .25V/DB IN 39 40 41 42 43 44 45 PWRSWP 46 47 48 49 50 .25V/DB B 51 52 53 54 PWR RAMPB 55 56 57 58 10V RAMPB 59 60 61 62 .25V/GHZB 63 64 65 66 FREQ RAMPB 67 68 69 70 71 72

U1 AD7547 — BD0 6, BD1 7, BD2 8, BD3 9, BD4 10, BD5 11, BD6 13, BD7 14, BD8 15, BD9 16, BD10 17, BD11 18, −10VR 4, FREQRAMP−+ 22, CSN0 5, CSN1 20, BUR/WN 19
U2 AD7547 — BD0 6, BD1 7, BD2 8, BD3 9, BD4 10, BD5 11, BD6 13, BD7 14, BD8 15, BD9 16, BD10 17, BD11 18, −10VR 4, −10VR 22, CSN2 5, CSN3 20, BUR/WN 19
U3 AD7547 — BD0 6, BD1 7, BD2 8, BD3 9, BD4 10, BD5 11, BD6 13, BD7 14, BD8 15, BD9 16, BD10 17, BD11 18, +10VR 22, CSN4 5, CSN5 20, BUR/WN 19

U4:A AD708 — C10 .01uF, C11 .01uF
U4:B AD708 — C4 33pF, C5 33pF
U5:A AD708 — C12 .01uF, C13 .01uF
U5:B AD708 — C6 33pF, C7 33pF
U6:A AD708 — C14 .01uF, C15 .01uF
U6:B AD708 — C8 33pF, C9 33pF
U7:A AD708 — C16 .01uF, C17 .01uF
U7:B AD708 — C78 .01uF
U9:A AD708 — C21 .01uF, C22 .01uF
U9:B AD708
U11:A AD708 — C30 .01uF, C31 .01uF
U11:B AD708 — C28 .01uF
U12:A TL072 — C25 .01uF, C26 .01uF
U12:B TL072
U13:A TL072 — C48 .01uF, C49 .01uF
U13:B TL072
U22:A AD708 — C50 .01uF, C51 .01uF
U22:B AD708
U23 AD587 — C46 .1uF, C47 10uF 50V

U8 LOG100 — K=5, K=3, K=1; C20 .01uF, C19 .01uF
U10:A IH5043 — C23 .01uF
U10:B IH5043
U14:A IH5043 — C29 .01uF
U14:B IH5043
U33:A IH5043 — C75 .01uF, C76 .01uF, C77 .01uF
U33:B IH5043

C1 .1uF, C2 .1uF, C3 .1uF
C27 .01uF, C32 47uF 25V, C33 47uF 25V, C34 47uF 25V, C36 .01uF

R1 10K, R2 10K, R3 1K, R5 10K, R6 4.99K, R7 NOM 15K, R8 10K, R9 10K, R10 1M, R11 100K, R12 1K, R13 10K, R14 100K, R16 100K, R17 10K, R18 10K, R19 10K, R20 10K, R21 10K, R22 100K, R23 10K, R24 10K, R56 10K, R57 10K, R71 10K, R72 10K, R73 4.99K, R74 10K, R75 10K, R76 3.32K, R77 10K, R78 162, R79 10K, R82 10K, R83 200

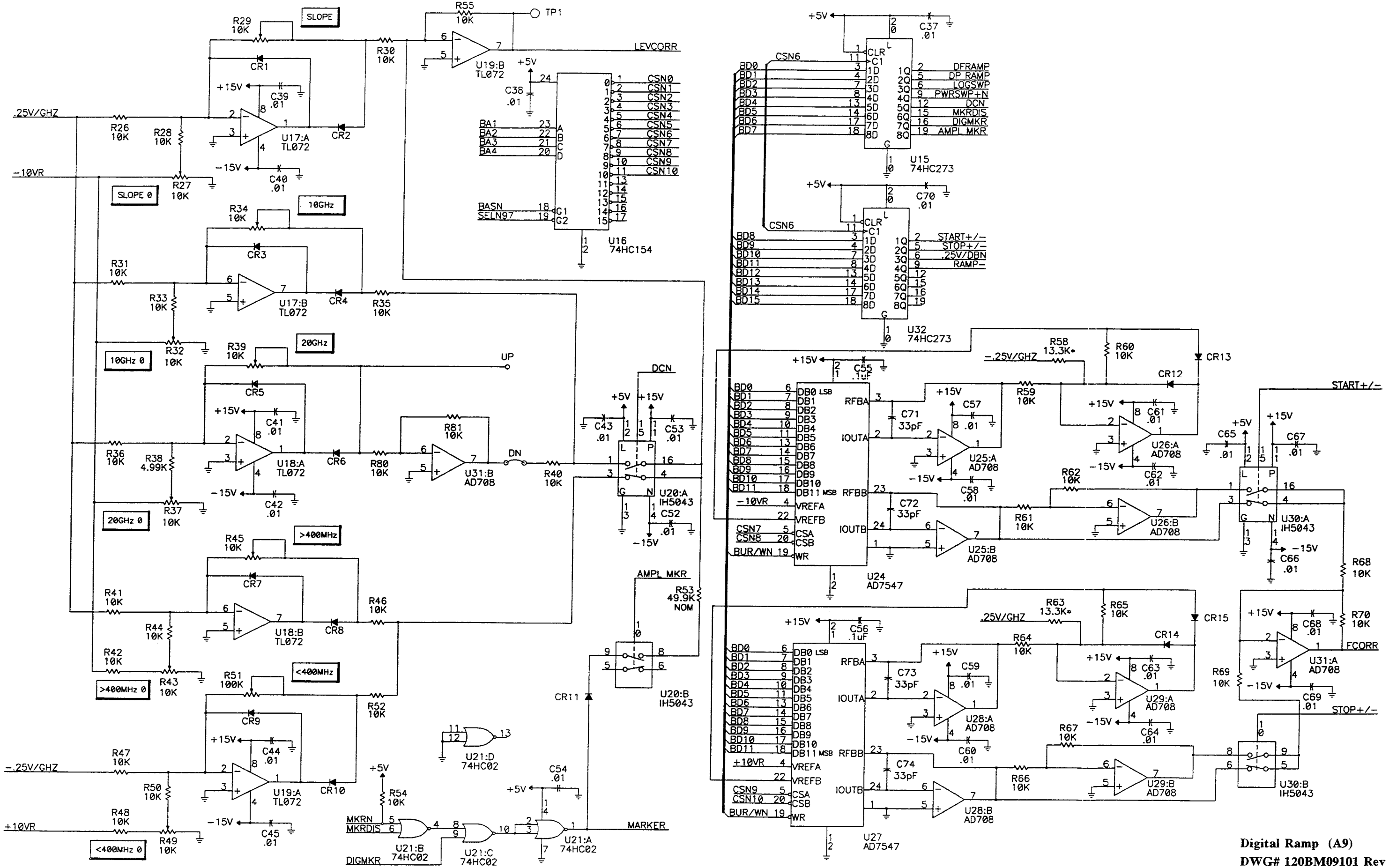
TP2, TP3

+15V, +5V, −15V, +10VR, −10VR, 10V RAMPB, DFRAMP, FREQ RAMPB, FREQRAMP−+, RAMP−, −.25V/GHZ, .25V/GHZ, .25V/GHZB, PWR RAMP, DP RAMP, .25V/DB IN, PWRSWP, LOGSWP, PWRSWP+N, .25V/DB B, PWR RAMPB, 10V RAMPB, .25V/GHZB, FREQ RAMPB, .25V/DBN

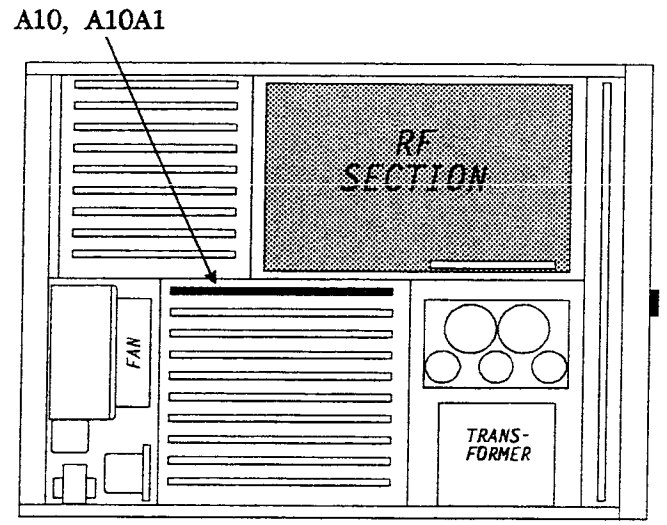
LIN, CAL, LIN SWEEP

NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/5W, 1%
4. * INDICATES 1/4W, 1% RESISTORS
5. DIODES ARE 1N4148

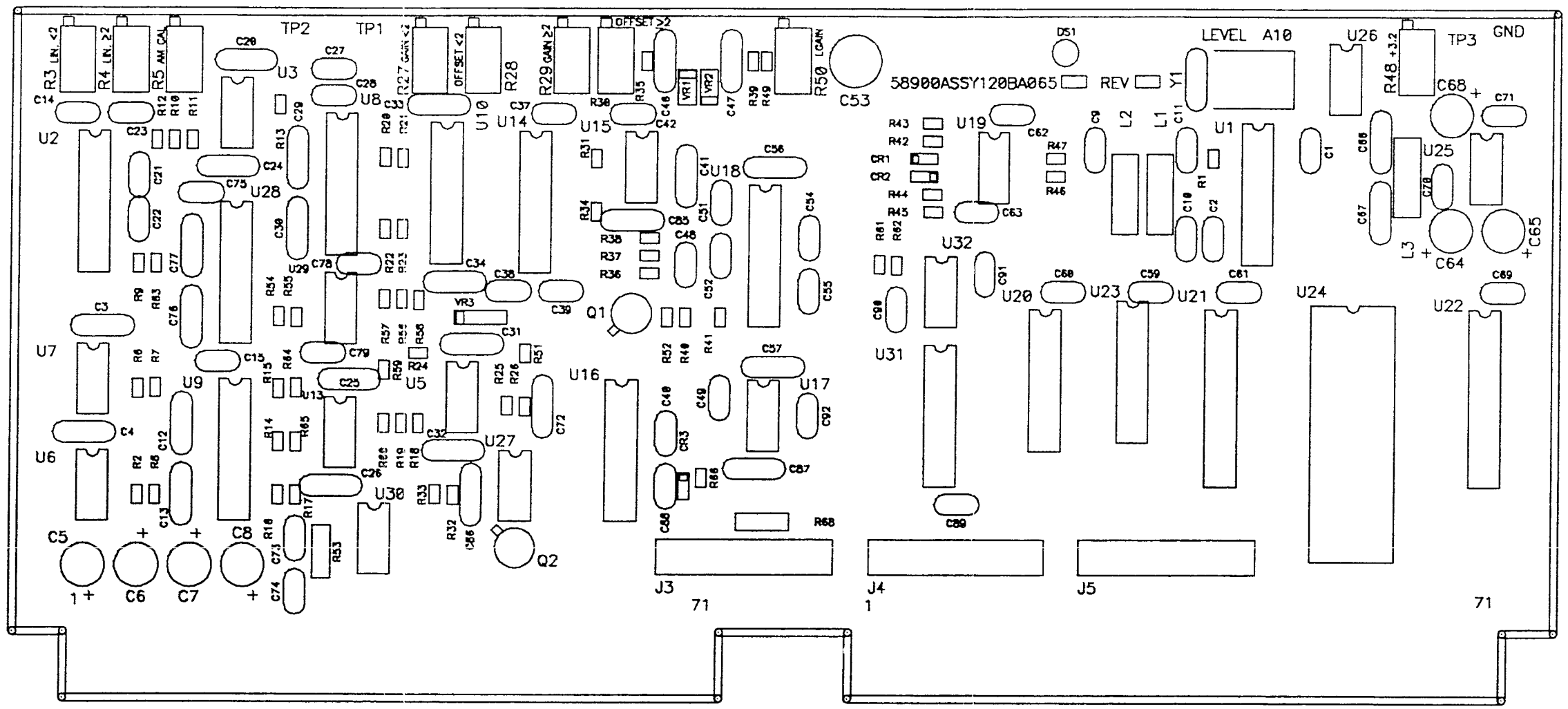
Digital Ramp (A9)
DWG# 120BM09101 Rev B
Sheet 2 of 3
7-A9-6



Digital Ramp (A9)
DWG# 120BM09101 Rev B
Sheet 3 of 3
7-A9-7



Level (A10)
ASSY# 120BA06510 Rev D
Sheet 1 of 5
7-A10-1



LEVEL -- PC ASSY A10

The leveling scheme used in the 7000 series can be compared to a Frequency Locked Loop. The similarities are that the leveling loop has a reference and a variable input which are compared and the loop action adjusts the variable input (which is proportional to the actual unit output level) until the two inputs are balanced. The comparison is made at the summing junction of an op amp integrator; the output of the integrator is used to control pin leveling diodes which adjust the RF power level. This power level is detected and amplified as required and is returned as the variable input to the integrator.

On this board U17 A is the op amp integrator whose summing junction at pin 2 is comparing a reference input and the detected RF input. The reference input is the REFX20 input from the detector buffer module A200 which is amplified by U15. The gain is adjustable via pots R27 (GAIN <2 for downconverter frequencies) and R29 (GAIN >2 for frequencies >2GHz) and is switched by U14 A and B depending on the instrument's output frequency. The variable input to the U17 summing junction is the actual RF detector voltage which has been amplified at the detector buffer module A200. Q2 samples this signal (DETX20) when the unit is pulse modulated. When the unit is not pulse modulated, Q2 is turned on and the detector voltage, buffered by U30, can be inverted by U27, depending on whether the detector voltage is negative or positive. This inversion is controlled by switch U16 A and B. In addition to these two inputs to the summing junction of U17, offset voltages are summed in as well. Two different adjustable offsets (R28 and R30) are available and are switched by U14 C and D depending on whether the output frequency is > or <2 GHz. Q1 samples the signals at this summing point when in pulse modulation mode or, if pulse is turned off, Q1 is turned on all of the time. The summing integrator U17 A has variable feedback paths available. U18 A, B, C and D are switched in as appropriate for different leveling modes. The output of the amplifier is fed to U19 via CR1 and CR2; this serves as a window detector to detect when the leveling loop is unleveled. When the loop is unleveled U19-7 goes low, lighting DS1 and sending a low logic signal to the computer. The output of the U17 A amplifier is also amplified by U17 B, whose gain is variable via R50 (LGAIN) pot. The output of U17 B is the level voltage which goes to the level driver board (A10A1) which ultimately drives the pin leveling diodes.

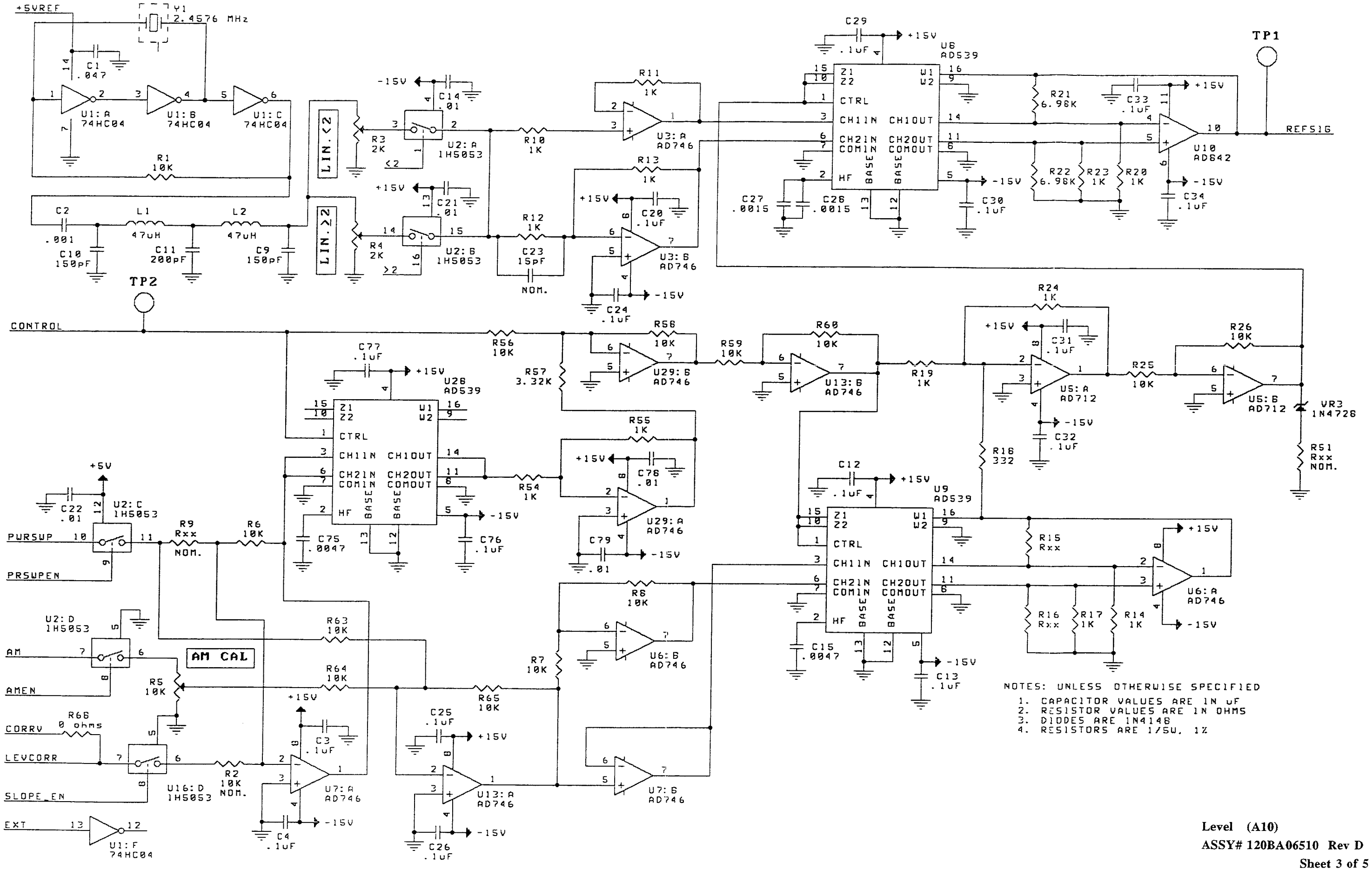
The reference signal is generated on this PCA. The 2.4596 MHz oscillator is composed of U1 A, B, C and Y1; its square wave output is then turned into a sine wave via filter L1, L2, C10, C11 and C9. R3 and R4 pots allow a variable amplitude of this signal to be tapped off and amplified. U2 A and B switch in the appropriate pot dependant on whether the frequency selected is > or < 2 GHz. The signal is translated into a differential signal and fed to a modulator U8 (which functions as a variable attenuator) controlled by a voltage which may be a composite of different signals. The output of the modulator is combined by U10 and is output to the Detector Buffer module to be amplified and returned to the leveling board as REFX20.

The main control voltage for the modulator IC's (U8, U28 and U9) is generated by the DAC U24. This voltage changes as the power level changes and is used to control the gain of U28. U28 adjusts the level correction voltage which is switched in by U16 D and amplified by U7 A. If power sweep is activated the power sweep ramp is enabled by U2 C and is also amplified by U7 A. The amplitude of these two signals is adjusted by the modulator U28 according to the power level the instrument is set to. U29 A amplifies the modulator output and sums it with the standard main control voltage at U29 B. The output of U29 B is inverted at U13 B and is used to control the modulator U9 which adjusts the amplitude of the AM signal when enabled by U2 D. R5 calibrates the AM signal which is then translated into a differential signal by U6 B and U7 B and applied to the modulator U9 input. The output of U9 is summed together by U6 A and this AM signal's amplitude has been adjusted according to the control voltage. The result is that the AM signal level is correctly calibrated for any power level. This AM signal is then summed together with its control voltage at U5 A and inverted at U5 B forming a composite signal used for appropriately modulating the reference signal at U8. VR3 and R51 are set to limit the control voltage so that it does not over drive the modulator.

U31 is a DAC programmed by the computer to give an output voltage at U32 B. This voltage is the appropriate offset required for the pin leveling diode drivers on the A10A1 level driver board.

The U26 Reference provides a 5 volt reference which is filtered by L3 and C66 and C67. This filtered 5 volt reference is also amplified by U32 A to give a 10 volt reference. The 5 volt reference is also divided down by pot R46 to give a 3.2 v reference.

U20 provides decoding for the chip select lines. U21, U22 and U23 provide the necessary buffers for the bus interface lines.



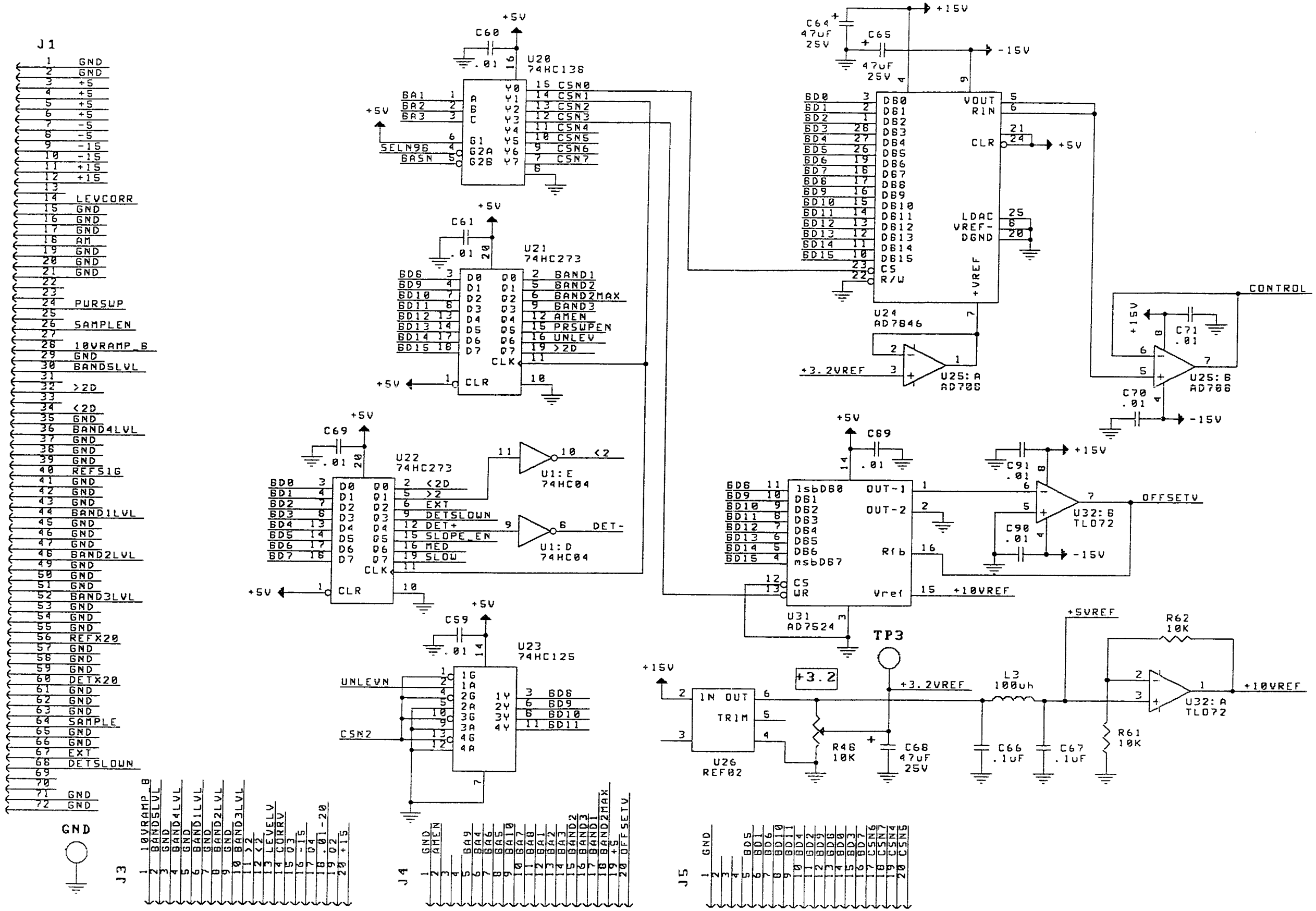
NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. DIODES ARE 1N4148
4. RESISTORS ARE 1/5W, 1%

Level (A10)
ASSY# 120BA06510 Rev D
Sheet 3 of 5
7-A10-3

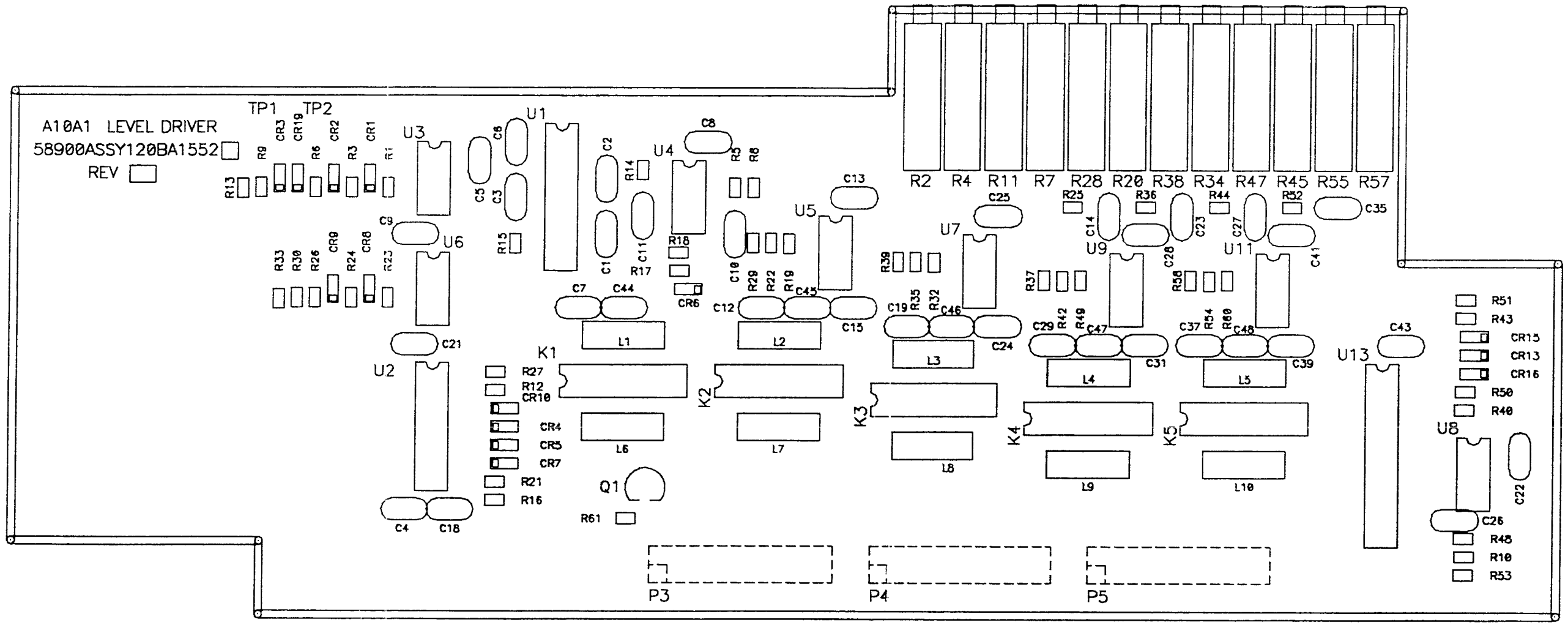
	<20 +		>20	
	AM	CW	AM	CW
.01-20	1	1	0	0
MED	0	1	0	1

+ 20.1 FOR UNITS X TO 20.1 GHz

Level (A10)
ASSY#120BA06510 Rev D
Sheet 4 of 5
7-A10-4

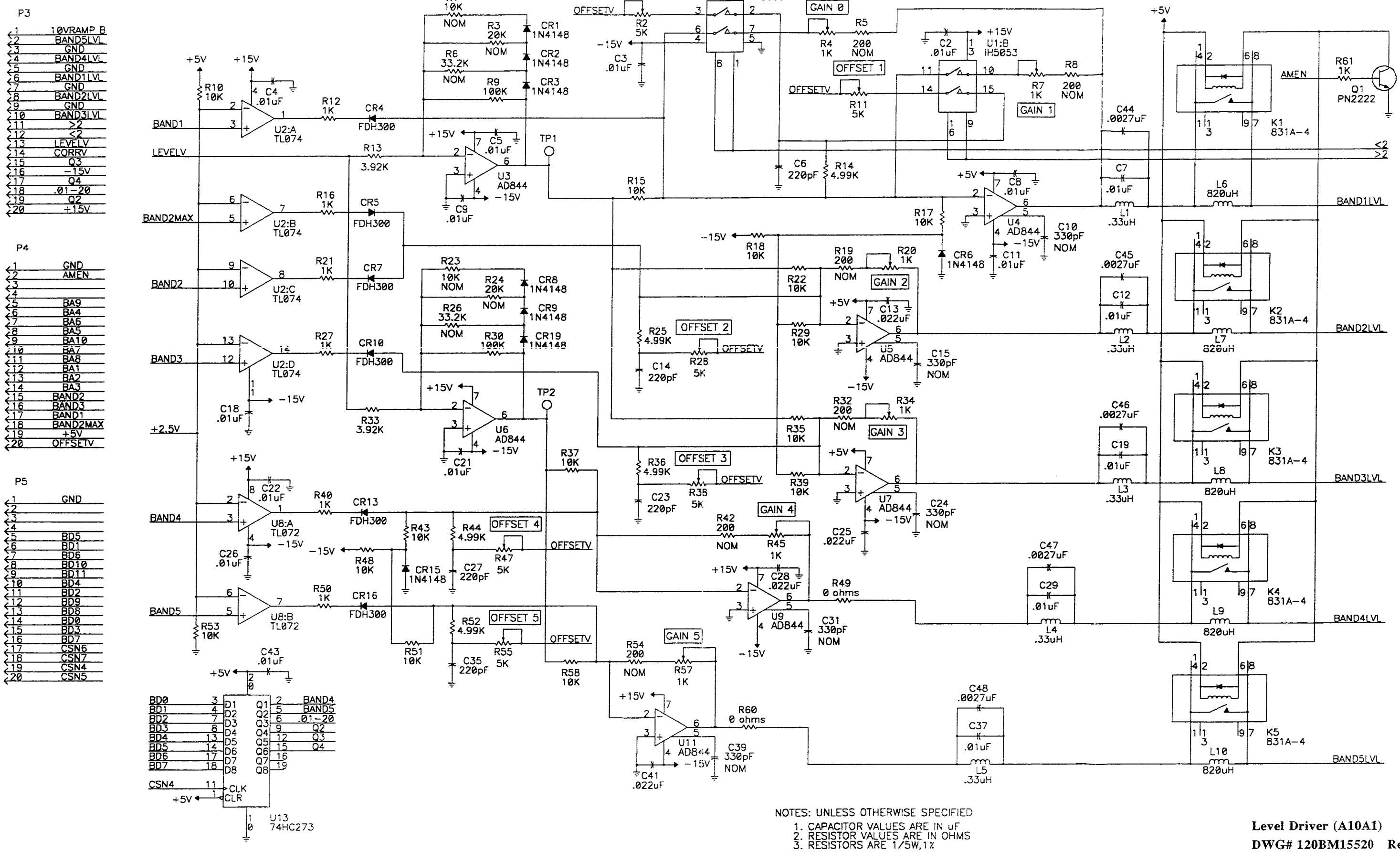


Level (A10)
ASSY#120BA06510 Rev D
Sheet 5 of 5
7-A10-5



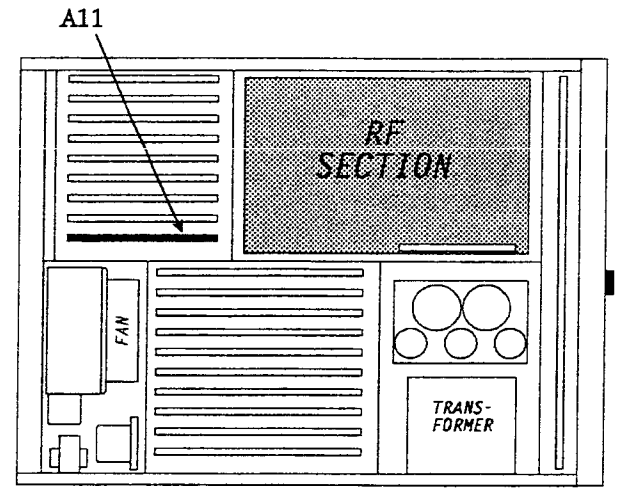
LEVEL DRIVER -- PC ASSY A10A1

The level driver board holds the circuits which directly drive the PIN diodes leveling circuits inside the RF modules. The level voltage which comes from the A10 level board is applied to the inputs of U3 and U6, which are variable gain amplifiers (their gain is dependent on the level of the input voltage). This variable gain is used to offset the gain change in the leveling loop caused by the leveling diodes. The outputs of U3 and U6 are applied to the summing junction inputs of inverting amplifiers U4, U5, U7, U9, and U11, each of which drives one leveler. Offset voltage inputs from PC board A10, amplified by U2 A through D and U8 A & B, are also applied to these summing junctions. The offset voltages vary, depending on output frequency, in order to keep the variable gain amplifiers within the correct range. The offset voltages are adjustable via pots R2, R11, R28, R38, R47, and R55. U1 changes the gain and offset for U4 when the output frequency is below 2 GHz.

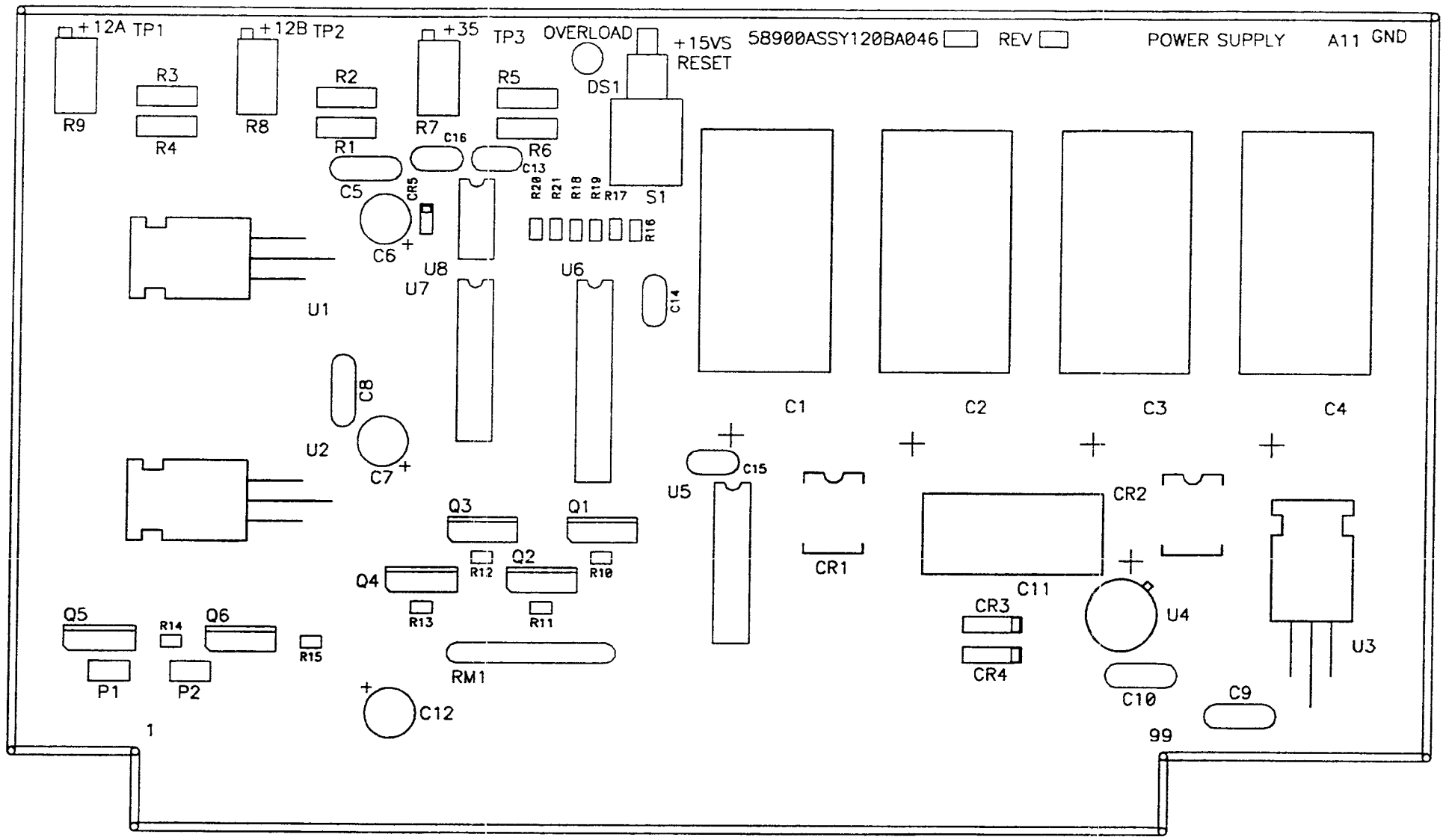


NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/5W,1%

Level Driver (A10A1)
DWG# 120BM15520 Rev A
Sheet 2 of 2
7-A10-7



Power Supply (A11)
DWG# 120BM04601 Rev C
Sheet 1 of 3
7-A11-1

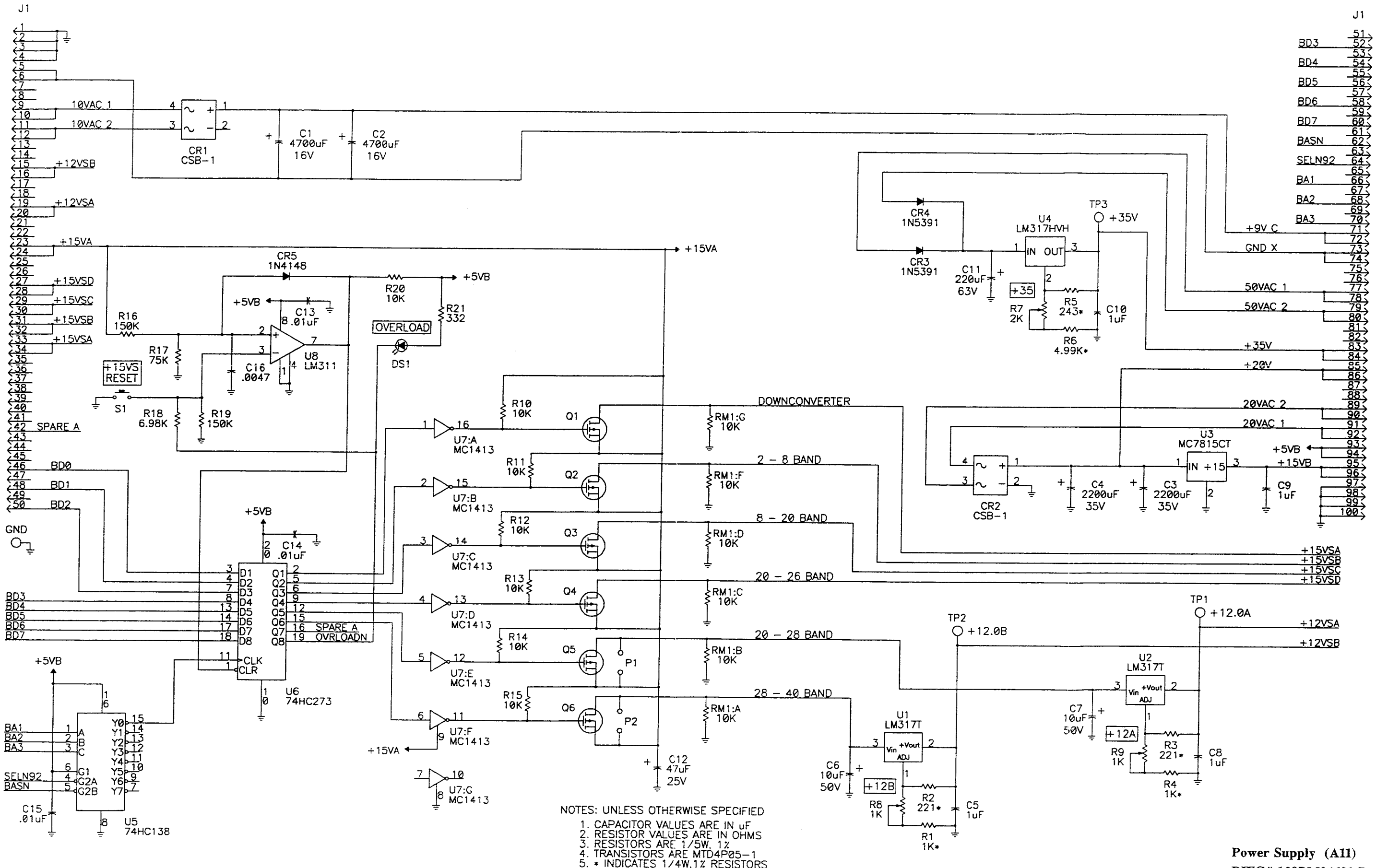


POWER SUPPLY -- PC ASSY A11

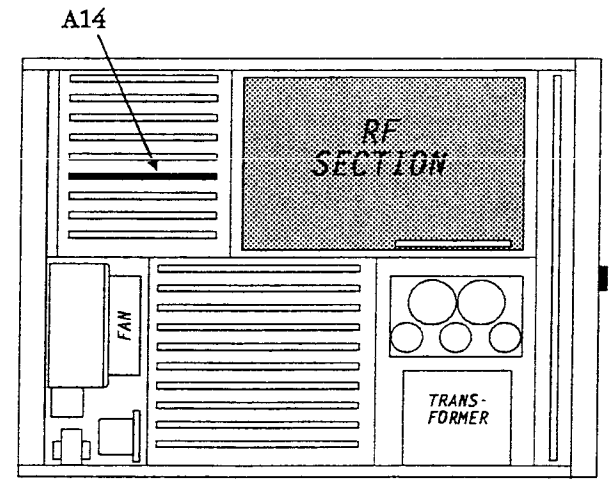
The A11 Power Supply PCA consists of several rectifiers, regulators, and FETs.

CR1 rectifies the 10 VAC from the power transformer to give approximately 9 volts output used for the front panel displays. CR2 rectifies 20 VAC, from the high stability transformer, to approximately 20 VDC. The 20 VDC is used to activate a relay when the power switch of the unit is turned on, and (after regulation by U3 to +15 V) is also used for the timebase oscillator and 100 MHz oscillator oven. The relay activates all of the internal power supplies of the instrument. CR3 and CR4 rectify 50 VAC from the transformer. The voltage is then regulated by U4 to +35 V for use by the front panel fluorescent displays.

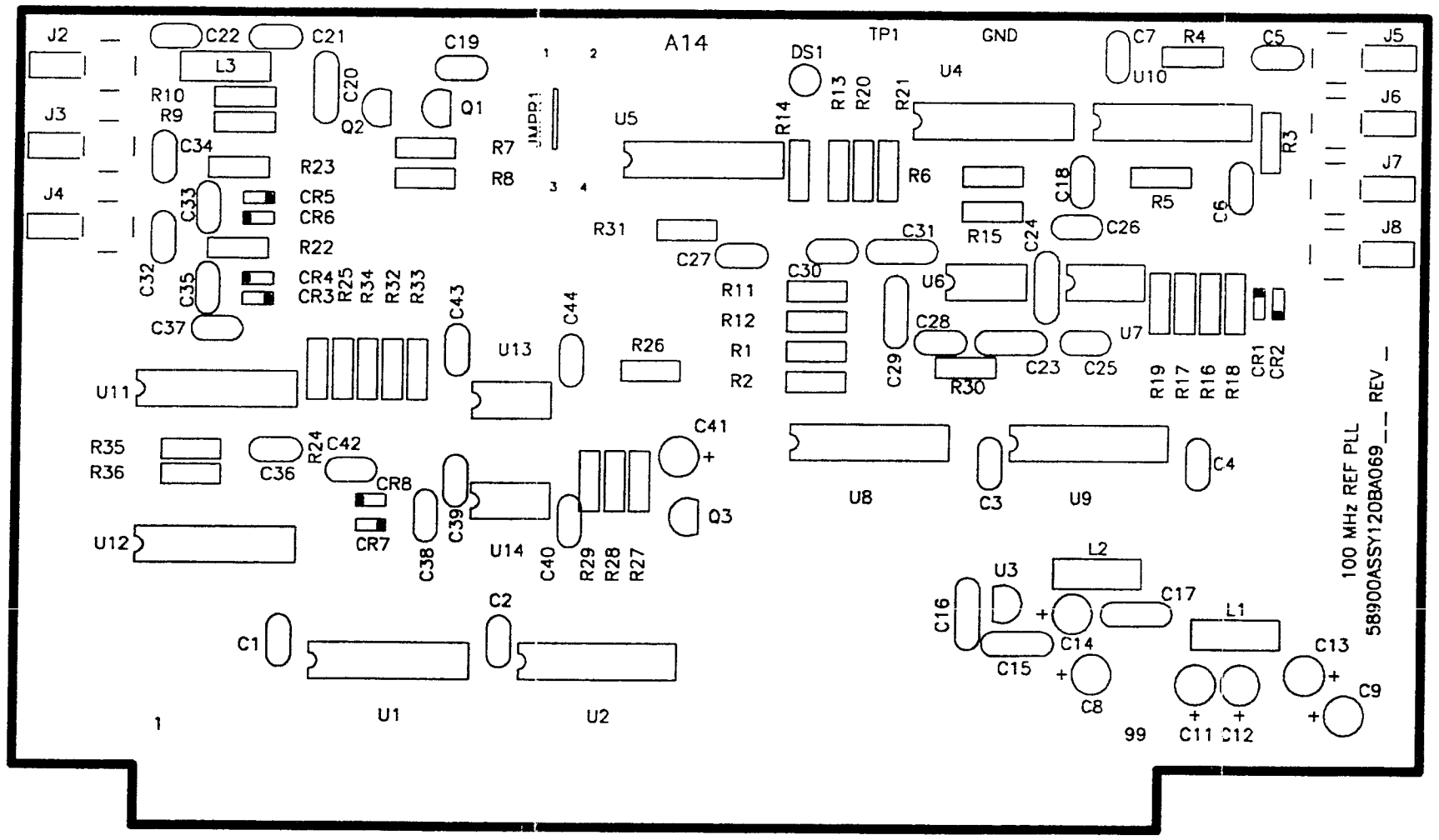
To avoid unnecessary consumption of power, voltage supplies to certain devices which are required only for particular frequency settings are switched. The switching circuit consists of U6, U7, and FETs Q1 through Q6. Q1 through Q4, when activated, furnish the +15 V supply to circuits required for operation in the Downconverter, 2-8, 8-20, and 20-26 frequency bands. In the 20-28 band, Q5 furnishes the +15 V supply to U2, which regulates it to +12 V for use by the 20-28 doubler circuit. In the 28-40 band, Q6 furnishes the +15 supply to U1, which regulates it to +12 V for use by the 28-40 doubler circuit.



Power Supply (A11)
DWG# 120BM04601 Rev C
Sheet 3 of 3
7-A11-3



100 MHz Ref PLL (A14)
DWG# 120BM06900 Rev B
Sheet 1 of 4
7-A14-1



100 MHZ REFERENCE PHASE LOCKED LOOP -- PC ASSY A14

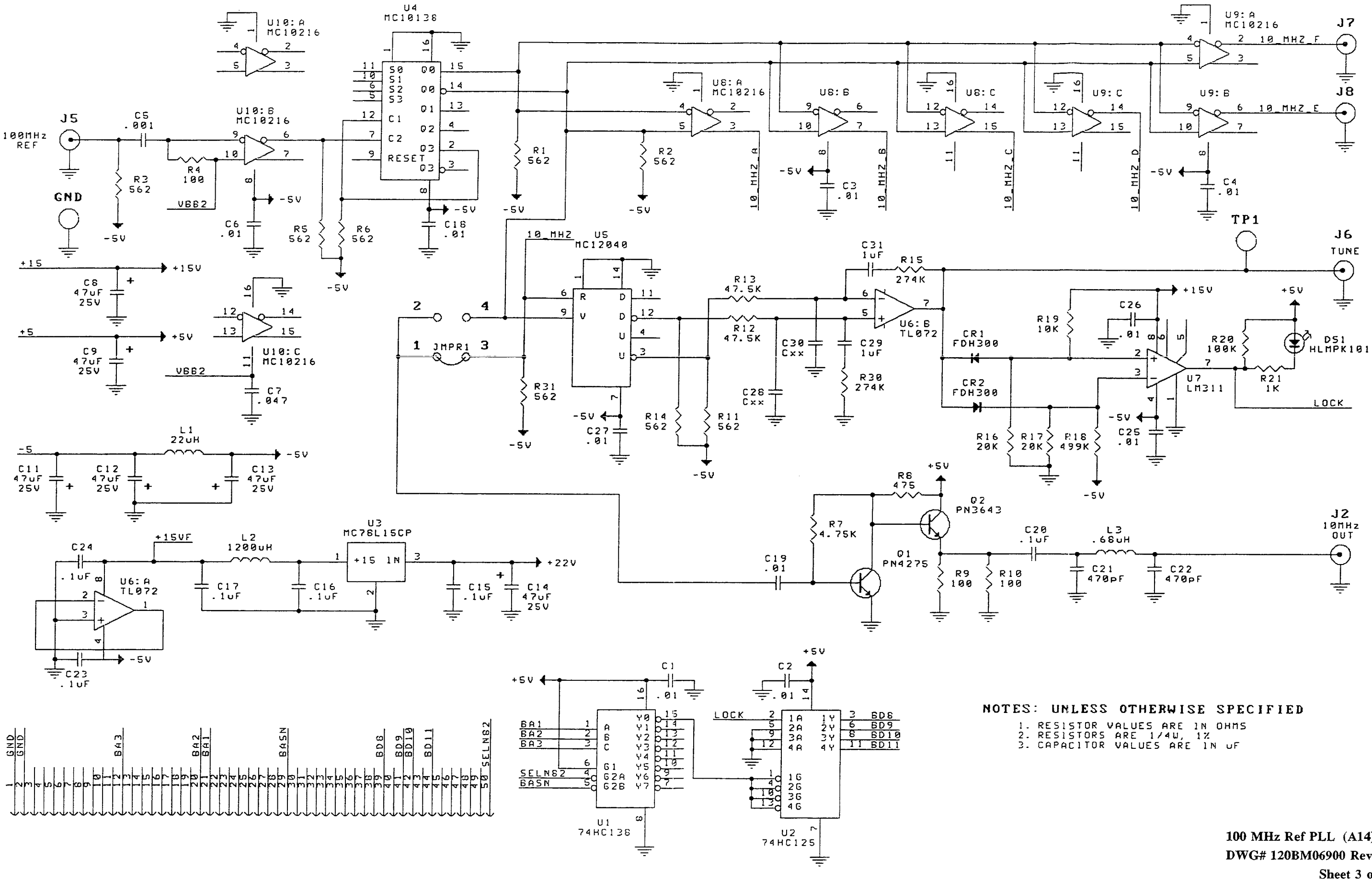
This circuit is used to phase lock the 100 MHz oscillator (A201) to the internal 10 MHz timebase or to an external timebase; in addition to the loop output it produces a lock indicator signal and a set of buffered 10 MHz outputs to be used for references for other loops in the instrument.

The 100 MHz input at J5 is buffered by U10 B before being divided down to 10 MHz by U4. This 10 MHz is then buffered by U8 A, B, C and U9 A, B and C so that it can be used by other circuits in the unit which require a 10 MHz reference. The signal is also applied to the variable input of the phase detector U5-9.

The reference input to the phase detector U5-6 comes from a switching circuit, which selects either an internal or external 10 MHz reference. When no external reference is present at J3 the internal 10 MHz reference at J4, buffered by U11 B, is allowed to propagate through U12 C and on to the phase detector (U5-6). When an external 10 MHz signal is present at J3 it is buffered by U11 A and allowed to propagate through U12 A to the phase detector. The presence of an external 10 MHz reference is detected when a charge is built up on C38 causing the switching circuit (comparator U14) to switch to a high state, in turn causing U13 output to go high which ultimately turns off the supply to the internal 10MHz reference. In addition, the switching circuit enables the external reference path at U12 A and disables the internal reference at U12 C. The selected reference is then available through Q1 and Q2 as the 10 MHz reference output on the rear panel.

The phase comparator U5 compares the 10MHz reference with the output of the divider U4 and determines which signal leads or lags the other. The output pulses at U5-12 and 3 are integrated or filtered by U6 B resulting in a tuning or correction voltage at J6 which will steer the 100 MHz VCXO oscillator in the proper direction (a more positive voltage increases frequency) to acquire and sustain a locked condition. When the loop is phase locked (the reference and variable input frequency and phase are equal) the output pulses of the phase detector will be extremely narrow at a 10 MHz rate. U7, CR1 and CR2 along with other components serve as a window detector which detects the tuning voltage and detects unlocked conditions. When the loop unlocks U7-7 goes low, lighting DS1 and sending the unlock logic level to the computer via U2, a tri-state buffer which serves as the interface to the bus. U1 is a 3 to 8 decoder which is used for decoding chip selects.

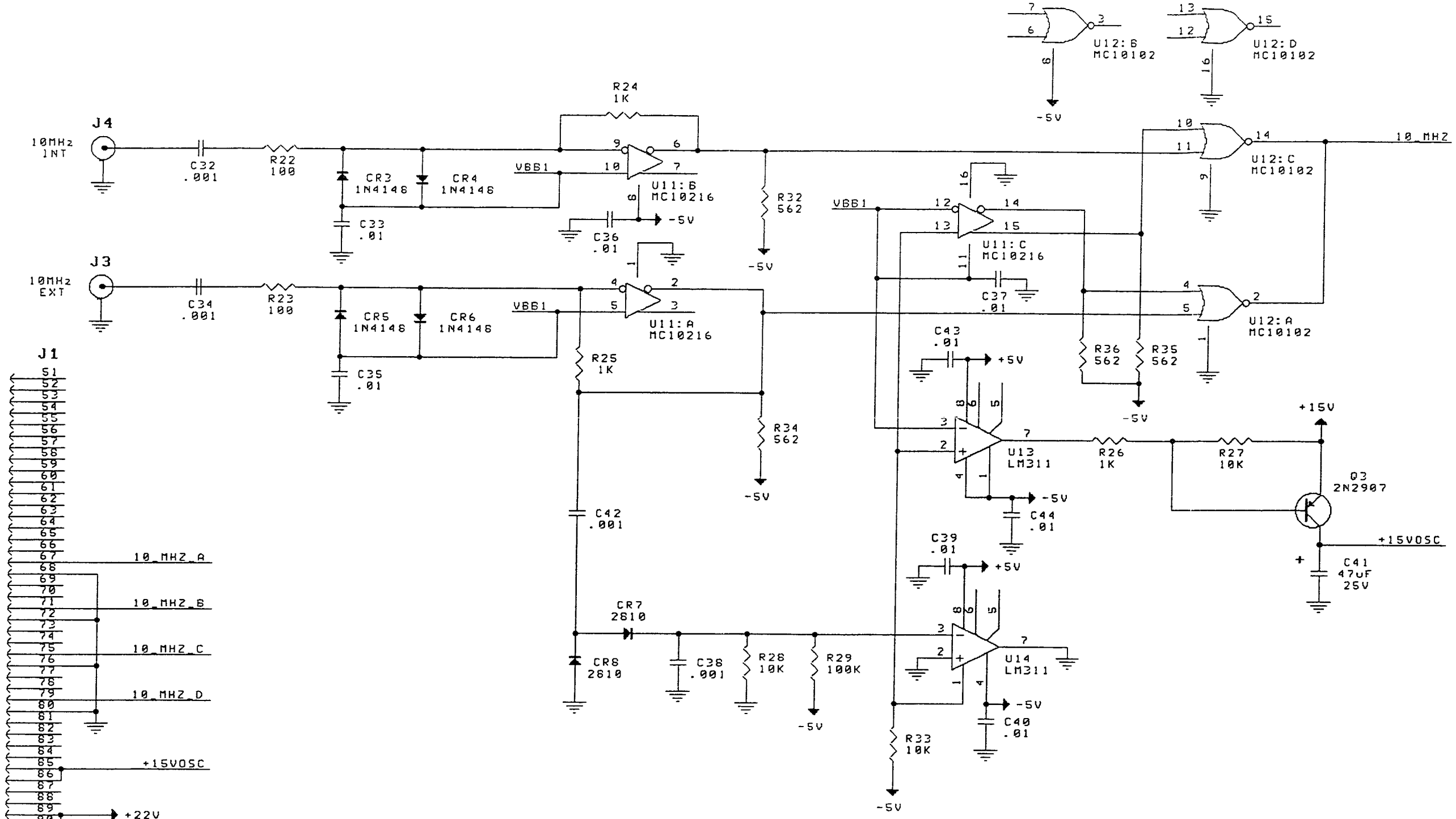
U3 regulates +22V to 15V which is then filtered by L1, C16 & 17 providing a clean supply for U6 thereby reducing noise introduced by the tuning voltage to the oscillator.



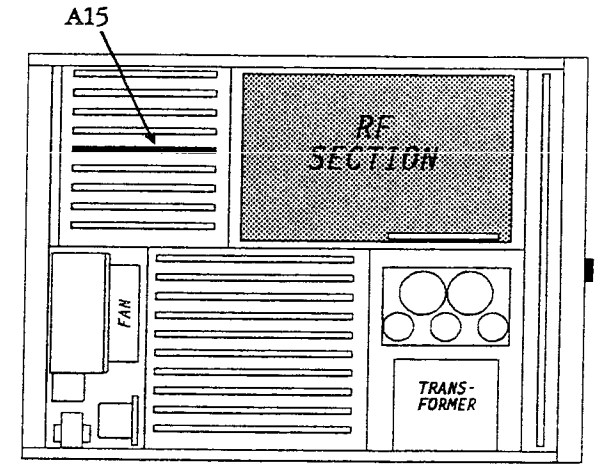
NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES ARE IN OHMS
2. RESISTORS ARE 1/4W, 1%
3. CAPACITOR VALUES ARE IN uF

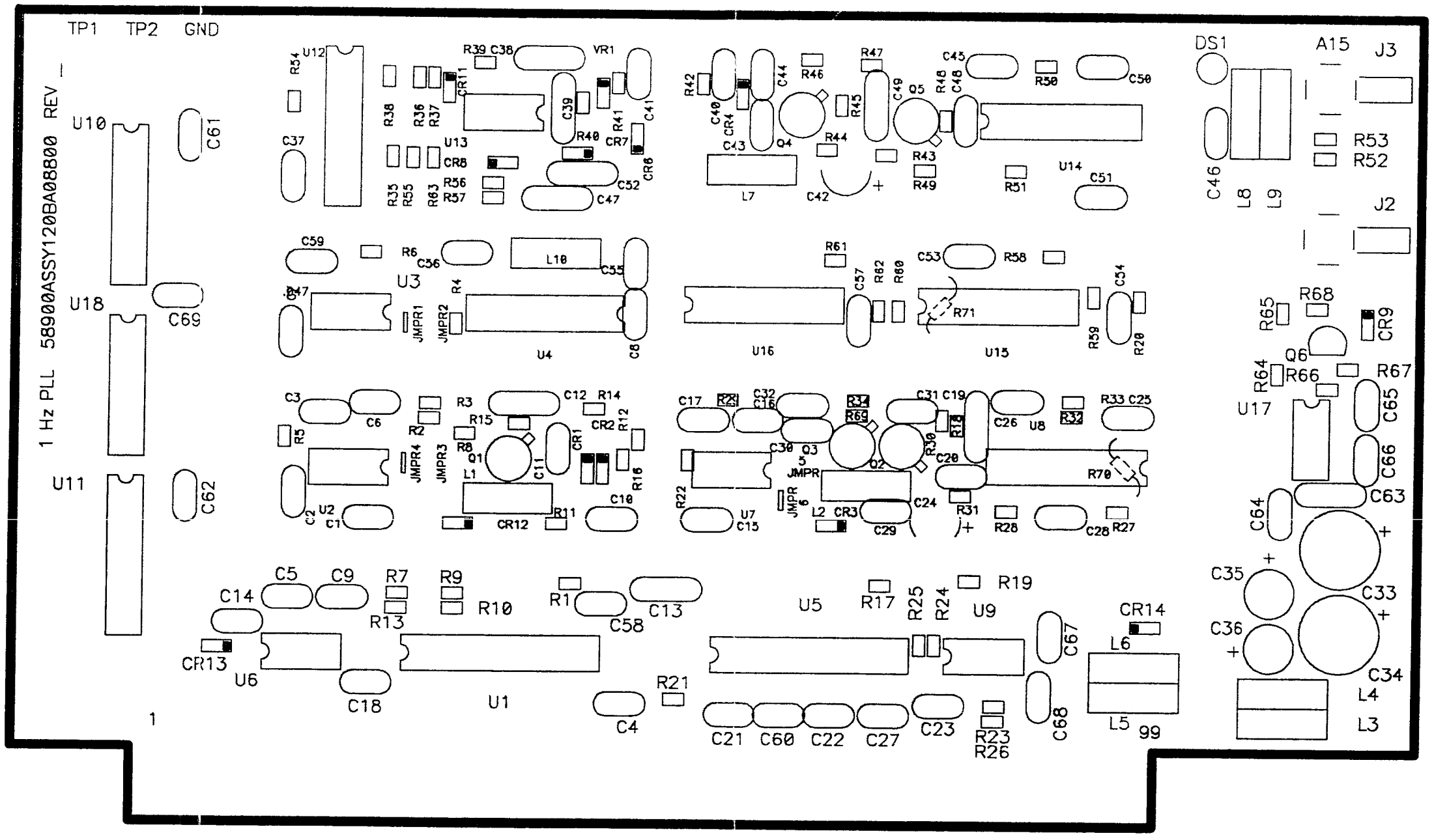
100 MHz Ref PLL (A14)
DWG# 120BM06900 Rev B
Sheet 3 of 4
7-A14-3



100 MHz Ref PLL (A14)
DWG# 120BM06900 Rev B
Sheet 4 of 4
7-A14-4



1 Hz Phase Locked Loop (A15)
ASSY# 120BA08800 Rev H



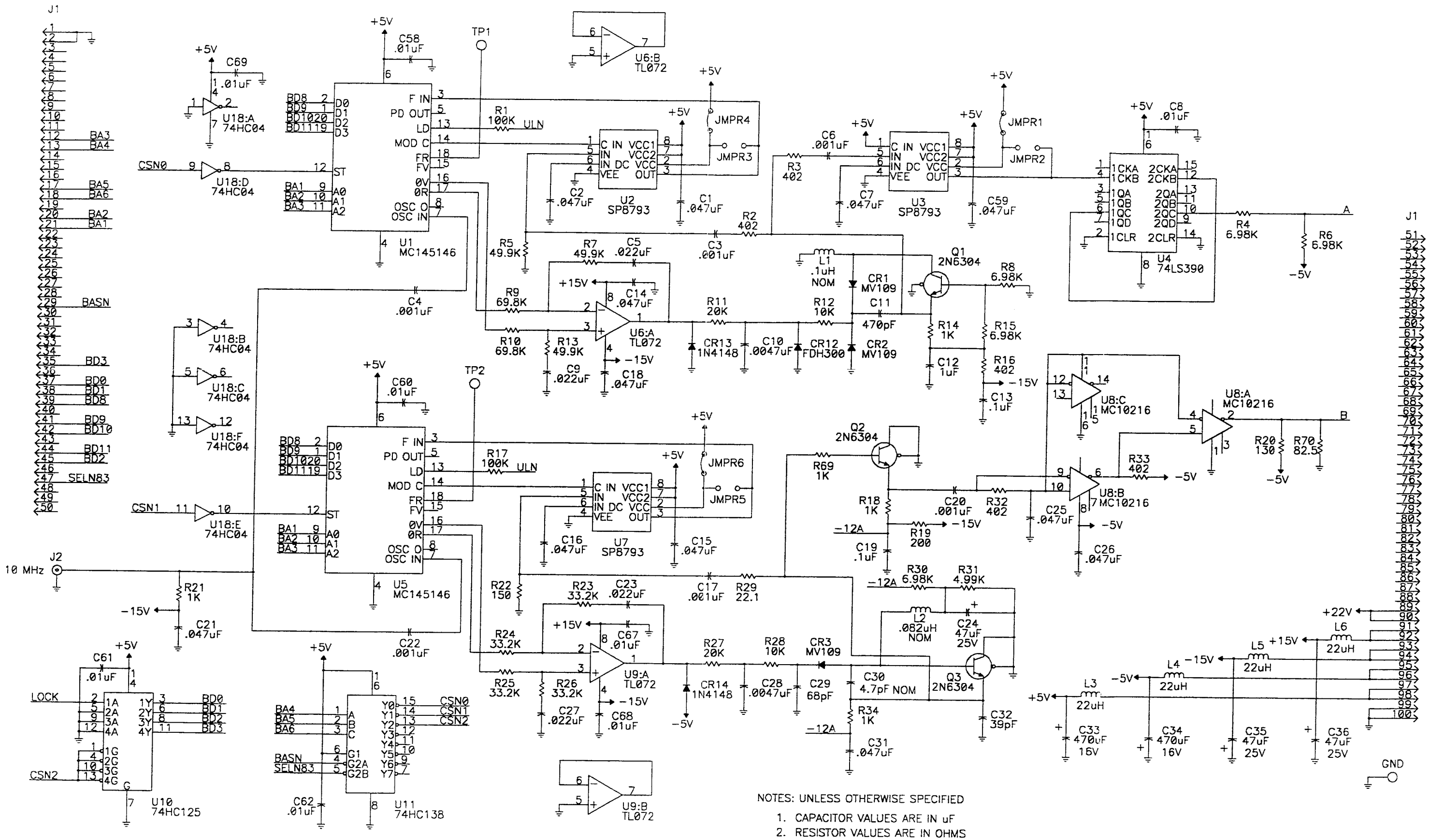
1 Hz PHASE LOCKED LOOP -- PC ASSY A15

This circuit synthesizes a reference frequency programmable in fine increments. This reference is substituted for the standard timebase signal used by the reference phase lock loop. By setting the reference output from this circuit, the computer is able to specify RF frequency in 1 Hz increments. The output at J3 has a range of 10-12 MHz and a resolution of 2 Hz; when divided in half at the reference PLL input, the result is a 5-6 MHz reference programmable in 1 Hz steps.

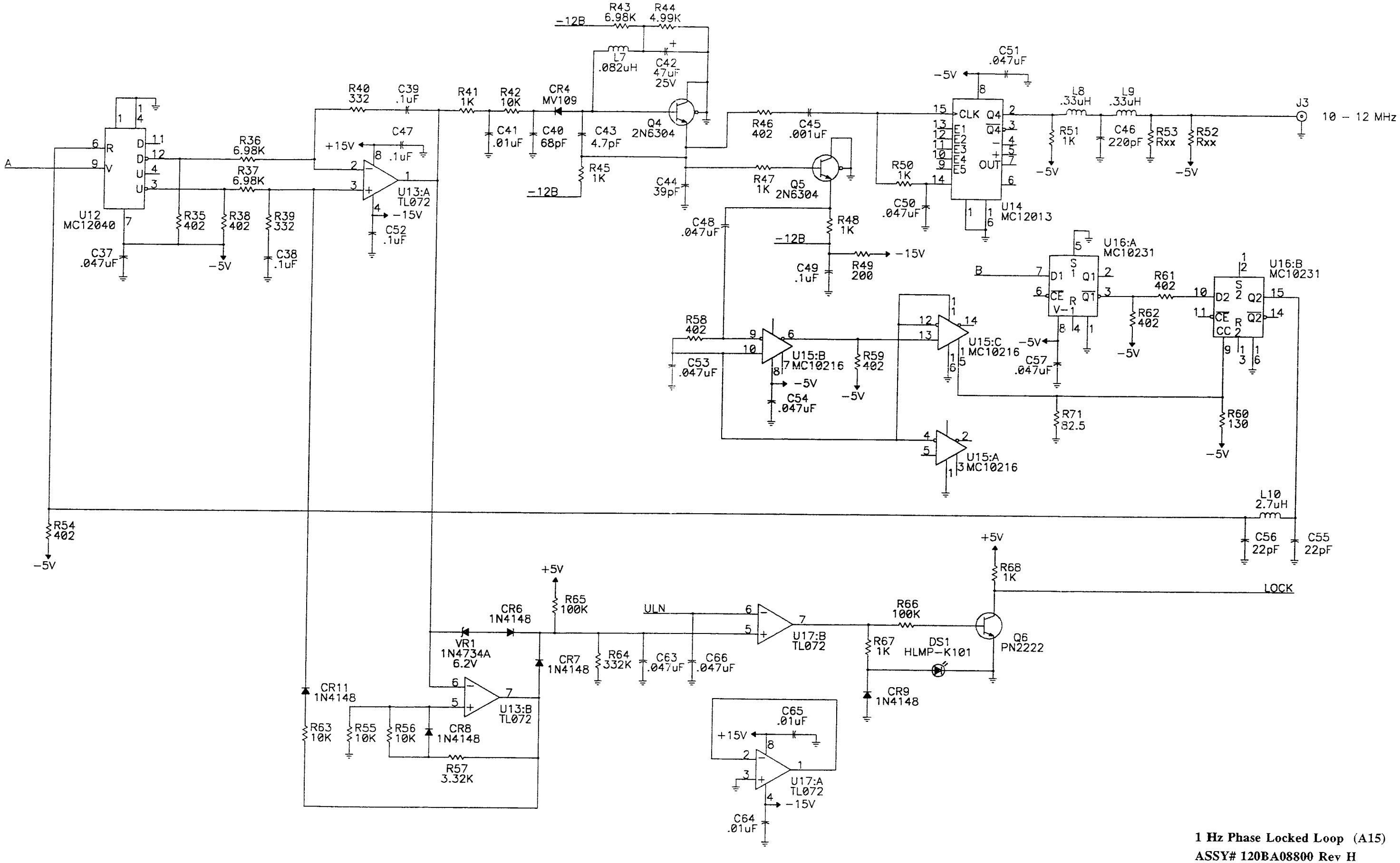
A 100-120 MHz voltage controlled oscillator (Q3) is controlled by U5. U5 is a synthesizer chip containing several programmable frequency dividers and a phase comparator, used in conjunction with an external prescaler (U7 which is programmed by U5 to divide by 40 or 41). U5 compares the prescaled feedback input from the VCO (U5-3) to the timebase input (U5-7) and produces pulsed outputs at U5-17 or U5-16 depending on which input is leading. A filter/amplifier circuit (U9 A) averages these pulses to produce a tuning input to the VCO. By programming the dividers in U5, the computer sets the VCO frequency in 50 kHz increments. The VCO frequency is buffered (Q2, U8 A and B) and applied to a mixer circuit consisting of the flip flops of U16.

The second frequency input to the U16 mixer circuit is produced by a second VCO (Q4) having the same range (100-120 MHz) but programmed in finer increments (20 Hz). This VCO is controlled by a PLL circuit consisting of a phase comparator (U12) and a filter/amplifier circuit (U13 A). The inputs to the phase comparator consist of feedback from the mixer circuit (U16-15) and a reference input from a third VCO circuit (Q1) divided down (by U3 and U4) to 100-150 kHz, giving 20 Hz increments. The PLL circuit phase locks the VCO to this reference. The circuit consisting of U13 B and U17 B performs as a window detector; when the PLL circuit is out of its normal control range, U17-7 goes high, illuminating the LED "unlock" indicator and pulling the 'LOCK' line low. The VCO output (from Q4) is divided by 10 (U14) yielding an output at J1 with a frequency range of 10-12 MHz and a resolution of 2 Hz.

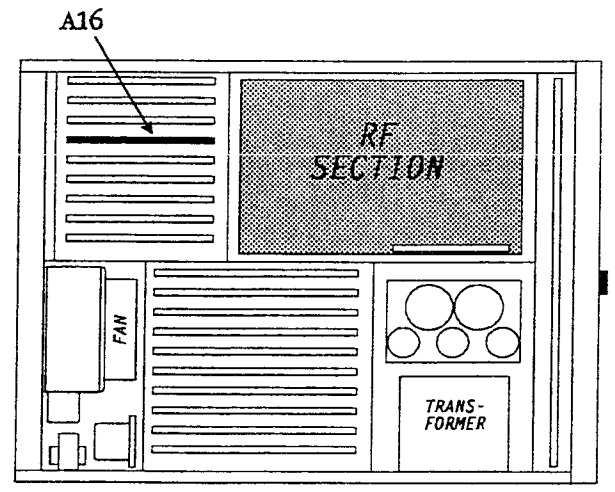
The third VCO (Q1) has a frequency range of 100-150 MHz, programmed in 20 kHz increments, but dividers U3 and U4 reduce this frequency to 100-150 kHz so that it can be used as a reference input by phase comparator U12. U1 is the same type of synthesizer chip as U5, and its prescaler chip U2 also divides by 40 or 41. Filter/amplifier circuit U6 A converts the phase comparator outputs of U1 into a tuning voltage for the VCO. U11 is a decoder chip used for decoding chip selects. U10 is a tri-state buffer for outputting board outputs to the bus.



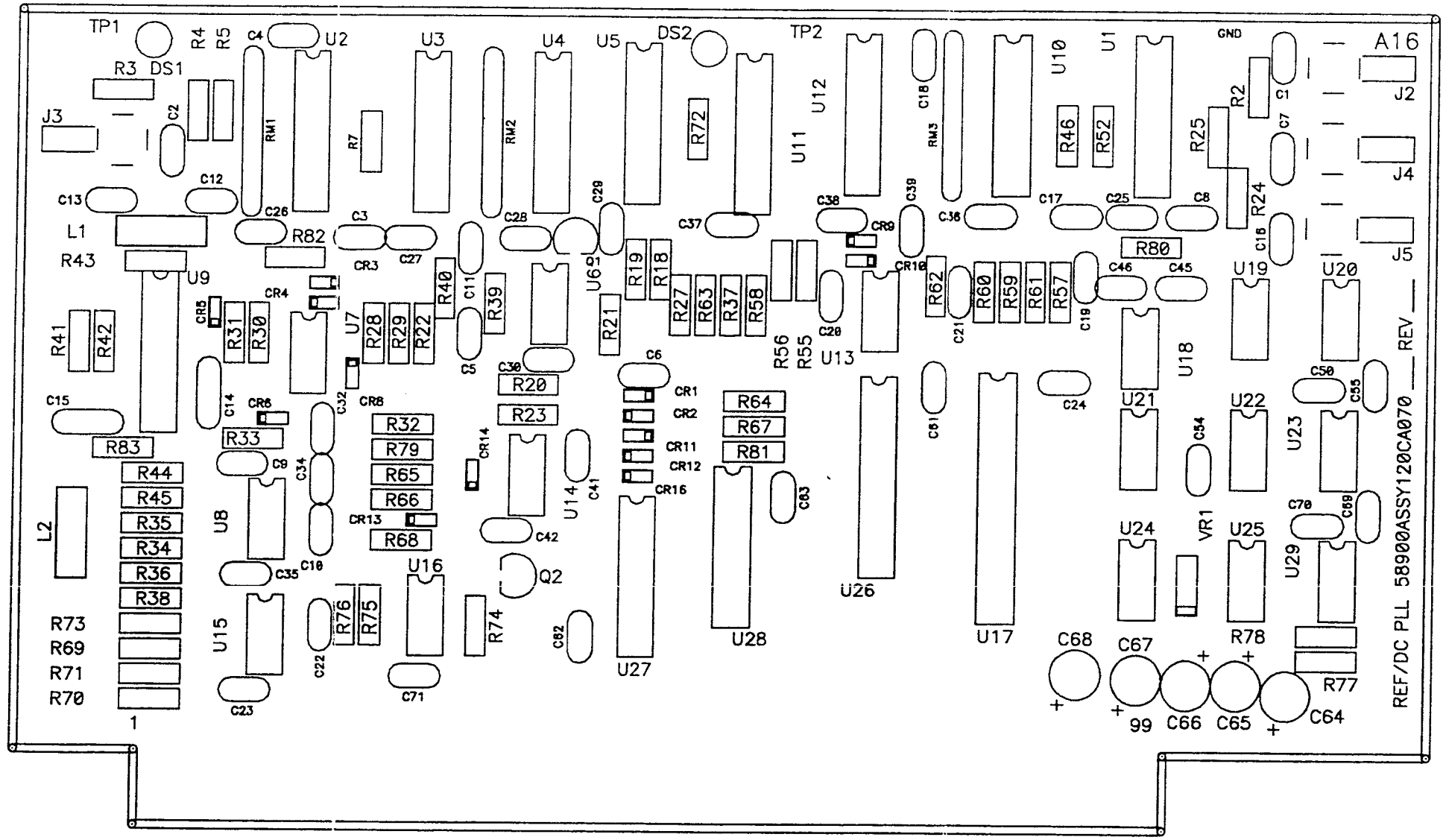
1 Hz Phase Locked Loop (A15)
ASSY# 120BA08800 Rev H
Sheet 3 of 4
7-A15-3



1 Hz Phase Locked Loop (A15)
ASSY# 120BA08800 Rev H
Sheet 4 of 4
7-A15-4



Ref/DC PLL (A16)
DWG# 120BM07000 Rev E
Sheet 1 of 5
7-A16-1



REFERENCE/ DOWNCONVERTER PHASE LOCKED LOOPS – PC ASSY A16

This board holds the Reference PLL, and the Downconverter (or Fixed LO) PLL circuitry as well as the logic and drivers for the Downconverter filters.

The REFERENCE PLL fine tunes the reference YIG oscillator in order to phase-lock it to a harmonic of the 100 MHz oscillator (see A201) and ultimately to the instruments timebase. The phase detector U5 compares two 5 MHz inputs, one from the reference sampler IF (J2), buffered by U1 C, and the other one from the internal or external input (J4 or J3 respectively). If the two 5 MHz inputs are out of phase, wide pulses will appear at one of U5's outputs (pins 3 or 12, depending on which input is leading). The filter/amplifiers (U6 A and B and associated components) convert these pulses into a correction voltage which is filtered by L1, C12 & C13 and then supplied to U9 which drives the fine tuning (or FM) coil of the reference YIG oscillator. The PLL circuit adjusts the frequency of the oscillator in whichever direction will reduce the phase difference between the two 5 MHz inputs. The PLL output goes more positive to increase frequency and more negative to decrease it.

The reference frequency is mixed with a 100 MHz comb line and should be 5 MHz **above** the 100 MHz multiple. If the reference frequency falls above the desired multiple, the output voltage at U6-1 will be higher than normal. The kicker circuit U7 A and associated components will detect this by comparing this voltage with a reference voltage set by R30, R31 and kick the output of U6 B high, resulting in the output of U6 A going low thus decreasing the oscillator frequency. On the contrary, if the output frequency is too low the kicker circuit U7 B and associated components will detect the output of U6 A being below a certain voltage level (set by R79, 32 and 33) and kick U6 such that the output at pin 1 will go high thereby increasing the output frequency.

Whenever the kicker circuits (U7) kick, C10 or C9 are charged up such that the lock detector U8 pulls the REF_LOCK signal low thereby illuminating the lock LED DS1.

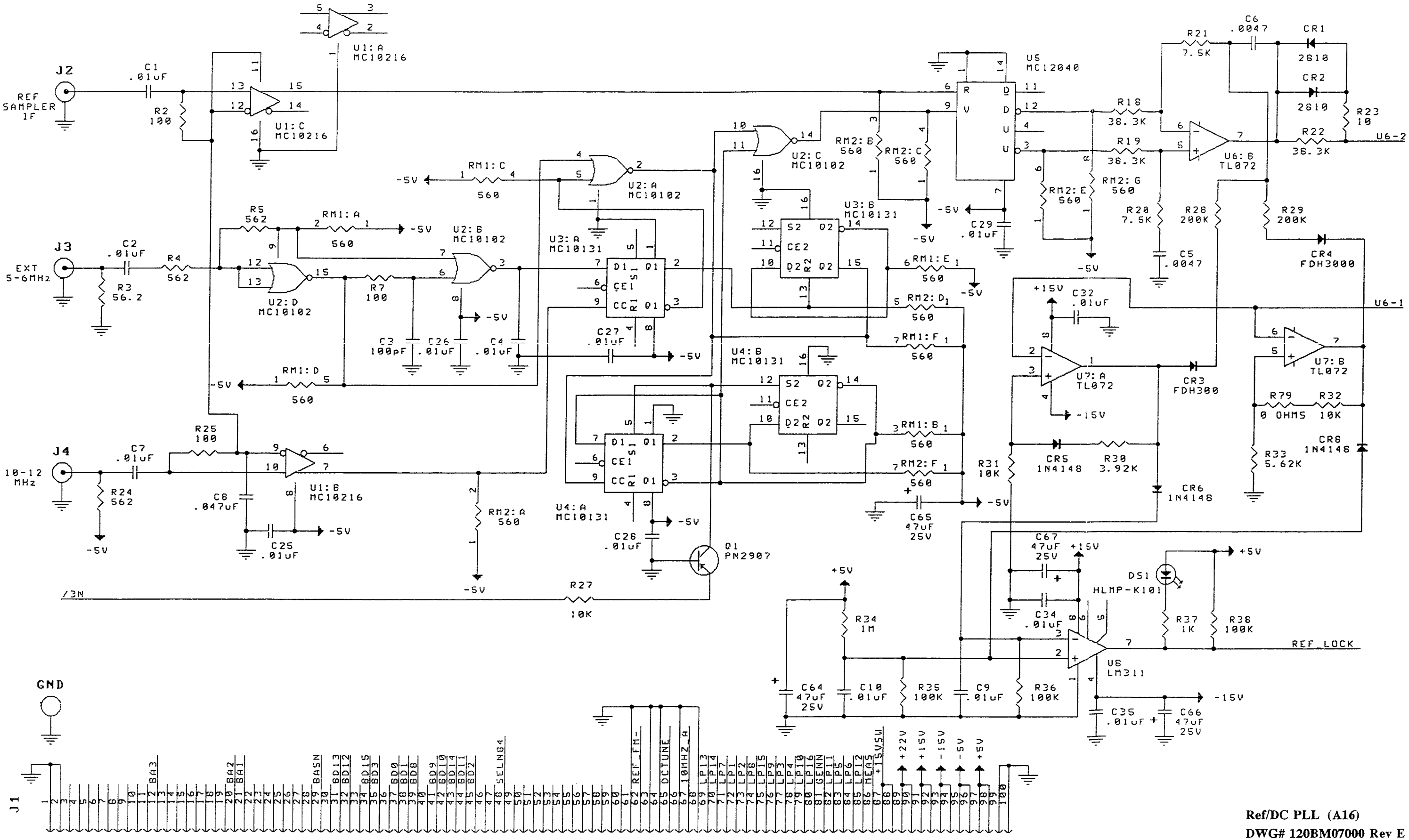
The 5 MHz input to the phase detector is derived either from the 10 MHz input at J4 or from the 5-6 MHz input at J3. The 5-6MHz input, if present must be detected so that the 10 MHz path will be disabled. This is achieved by delaying one input to U2 B using R7 an C3. This causes U2-3 output to be low thus disabling the 10 MHz from propagating thru U3 A. Instead the 5-6 MHz input propagates thru to the phase detector U5. When no 5-6 MHz input is present the 10 MHz propagates thru U3 A and B, being divided by two, and then on thru U2 C to the phase detector input.

At some output frequencies the sampler IF is 1.667 MHz rather than 5 MHz; in that situation the control input at Q1 causes the flip flop U4 to be activated which removes two pulses out of every three coming from either U2-2 or U3-15. This effectively divides the 5 MHz by three which yields the desired 1.667 MHz signal.

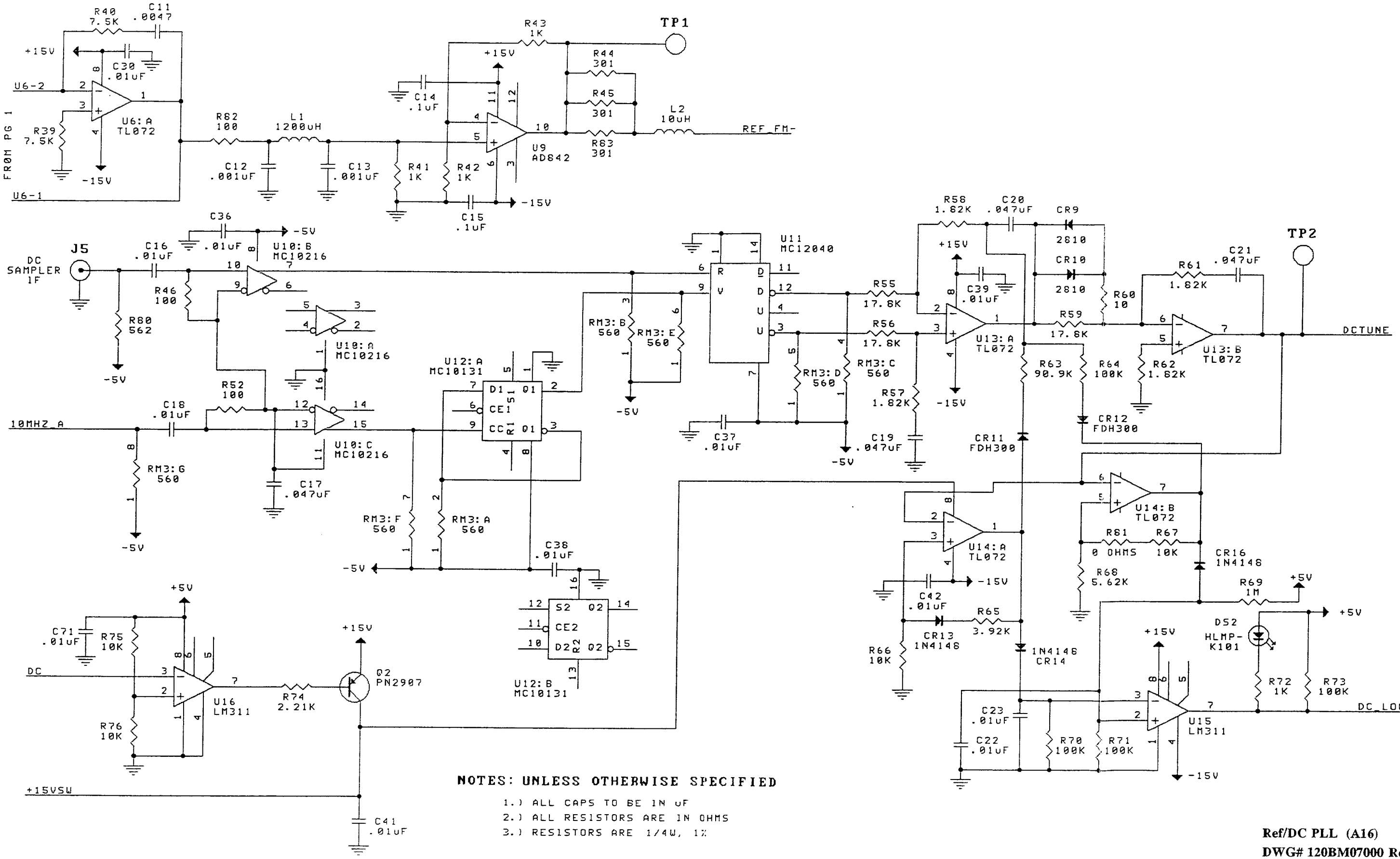
The DOWNCONVERTER PLL (or Fixed LO PLL) circuitry functions basically identical to the Reference PLL. One difference is that there is only one set of inputs to the phase detector U11, the 10 MHz and the DC sampler IF. When the loop is locked the DC sampler IF should be 5 MHz, the flip flop U12 divides the 10 MHz reference by two yielding 5 MHz. The other difference is that this loop is turned off by U16 and Q2 when the unit is not operating in the downconverter range. This reduces spurs and noise which can be added by this circuitry when it is not locked.

This board also provides downconverter filter drive logic. U17 is a 4 to 16 decoder which decodes logic from the computer there by selecting each of the downconverter filters as appropriate via their drive circuitry U18 thru U25. The GENN and MEAS logic drives for the computer are provided by U29.

U27 provides chip selects for various IC's on the board and U26 and U28 serve as buffers required for computer bus interface.



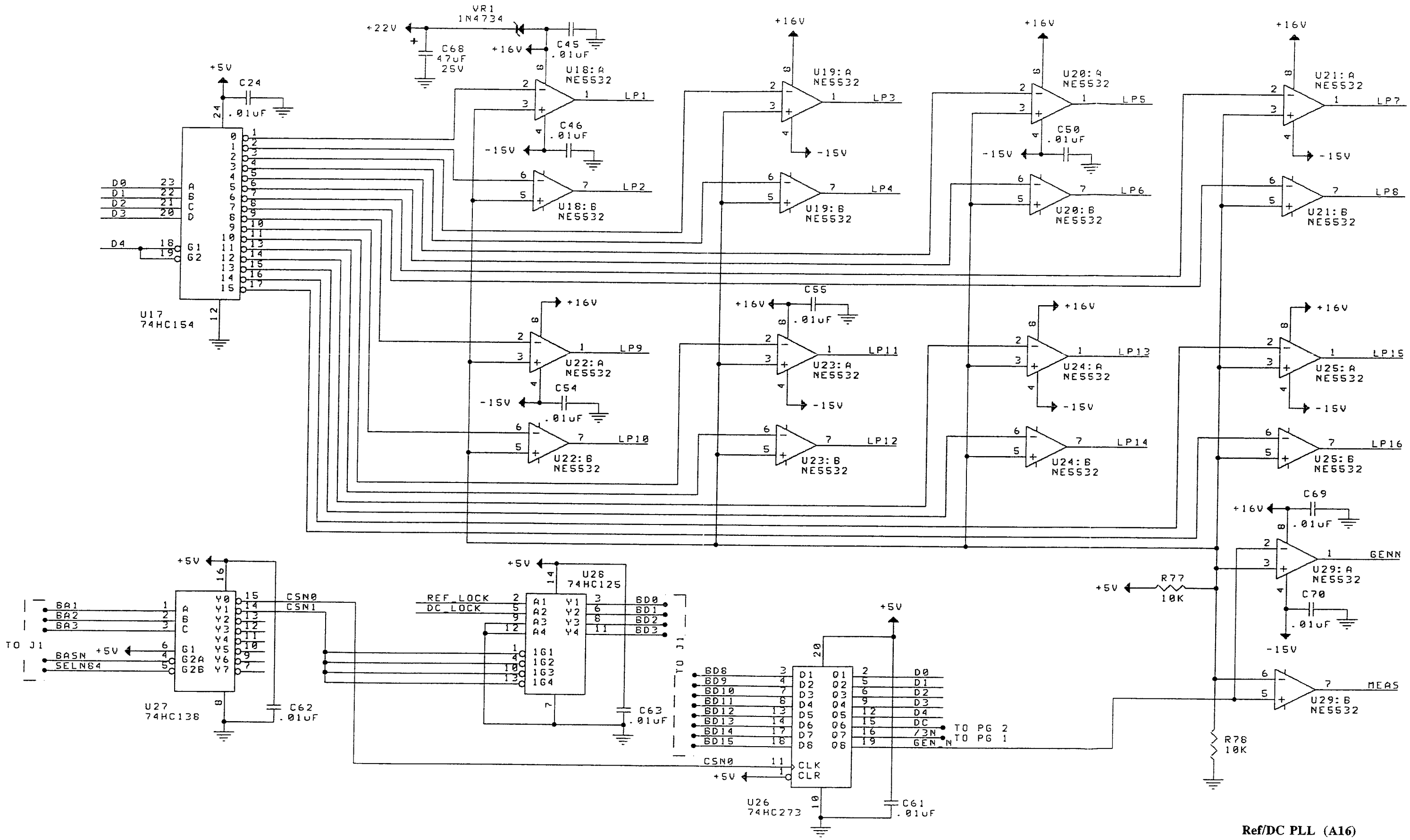
Ref/DC PLL (A16)
DWG# 120BM07000 Rev E
Sheet 3 of 5
7-A16-3



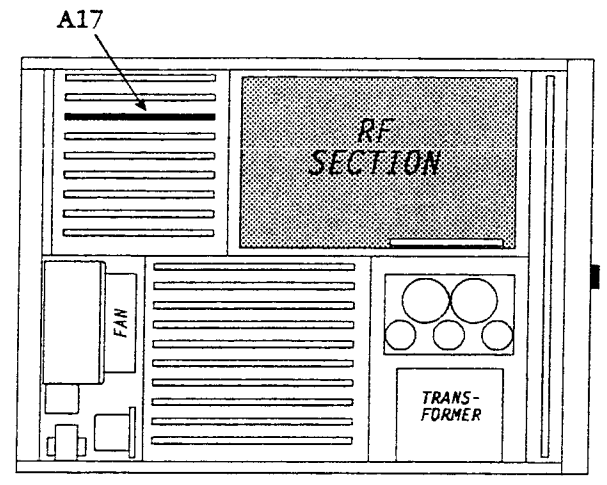
NOTES: UNLESS OTHERWISE SPECIFIED

1.) ALL CAPS TO BE IN uF
2.) ALL RESISTORS ARE IN OHMS
3.) RESISTORS ARE 1/4W, 1%

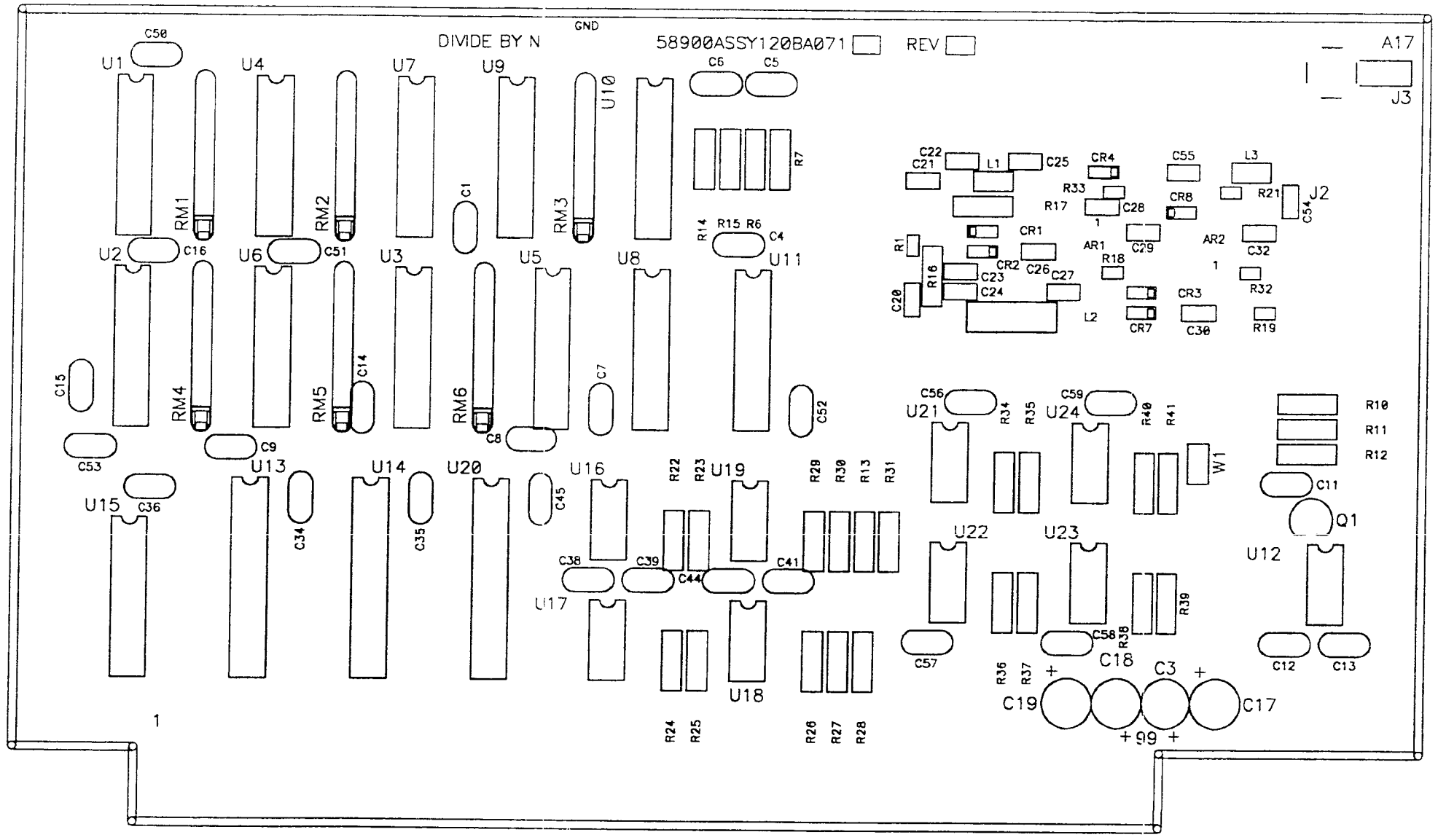
Ref/DC PLL (A16)
DWG# 120BM07000 Rev E
Sheet 4 of 5
7-A16-4



Ref/DC PLL (A16)
DWG# 120BM07000 Rev E
Sheet 5 of 5
7-A16-5



Divide By N (A17)
ASSY# 120BA07100 Rev H
Sheet 1 of 5
7-A17-1



DIVIDE BY N – PC ASSY A17

This circuit is a programmable frequency divider. It is set by the computer with a divisor between 95 and 395. Its frequency input is the 95 to 395 MHz I.F. from the reference mixer. The divided I.F. is supplied to the output phase lock loop and should be exactly 1 MHz when the output loop is locked. A 2 stage amplifier is used to provide enough gain throughout the operating frequency range to drive the Mod-8/9 counter (U11). AR1 and AR2 are amplifiers. CR1,2 and C23 detect the level of the signal at the output of AR1 and U12 A and Q1 provide bias to CR6, CR5, CR3 and CR4 to attenuate the signal as required, thereby providing a form of automatic level control. L2, C24 and C27 are required for power supply filtering. L3, C54, C55, and L1, C25, C22 are low pass filters to filter the IF signal.

In the discussion of the divider circuit, terms are defined as follows: "I.F. cycles" refers to the amplified I.F. from the reference mixer, which is used as a timing clock by the Mod 8/9 counter; "clock cycles" refers to the output of the Mod 8/9 counter, U11-2, which is used as a timing clock by the three-bit and six-bit counters; "division cycles" refers to the output signal, U9-14, which should have a rate of 1 MHz when the loop is locked. I.F. cycles are the fastest of the three; division cycles are the slowest.

The divisor, selected by the computer, is supplied as a nine-bit binary number at TTL levels to the 10124 translators (U1, 2 and 3), which convert the bits to ECL levels. Bits 0, 1 and 2 control the three-bit counter (U5) and bits 3 through 8 control the six-bit counter consisting of U4, 6 and 7. These two counters operate independently, but they use the same timing clock and they count down simultaneously.

The outputs of the three-bit counter U5, by way of gate U8, program the Mod- 8/9 counter U11 ; while U5 is counting down, U11 divides the I.F. by 8. In the case of most divisors, it is necessary for the I.F. to be divided by 9 for some portion of the division cycle; only when the three lowest bits are all zero is U11 programmed as a Mod-8 counter throughout the division cycle (a situation which can only occur if the divisor itself happens to be an even multiple of eight). Whenever it reaches zero, U5 stops counting until it is preset at the next division cycle.

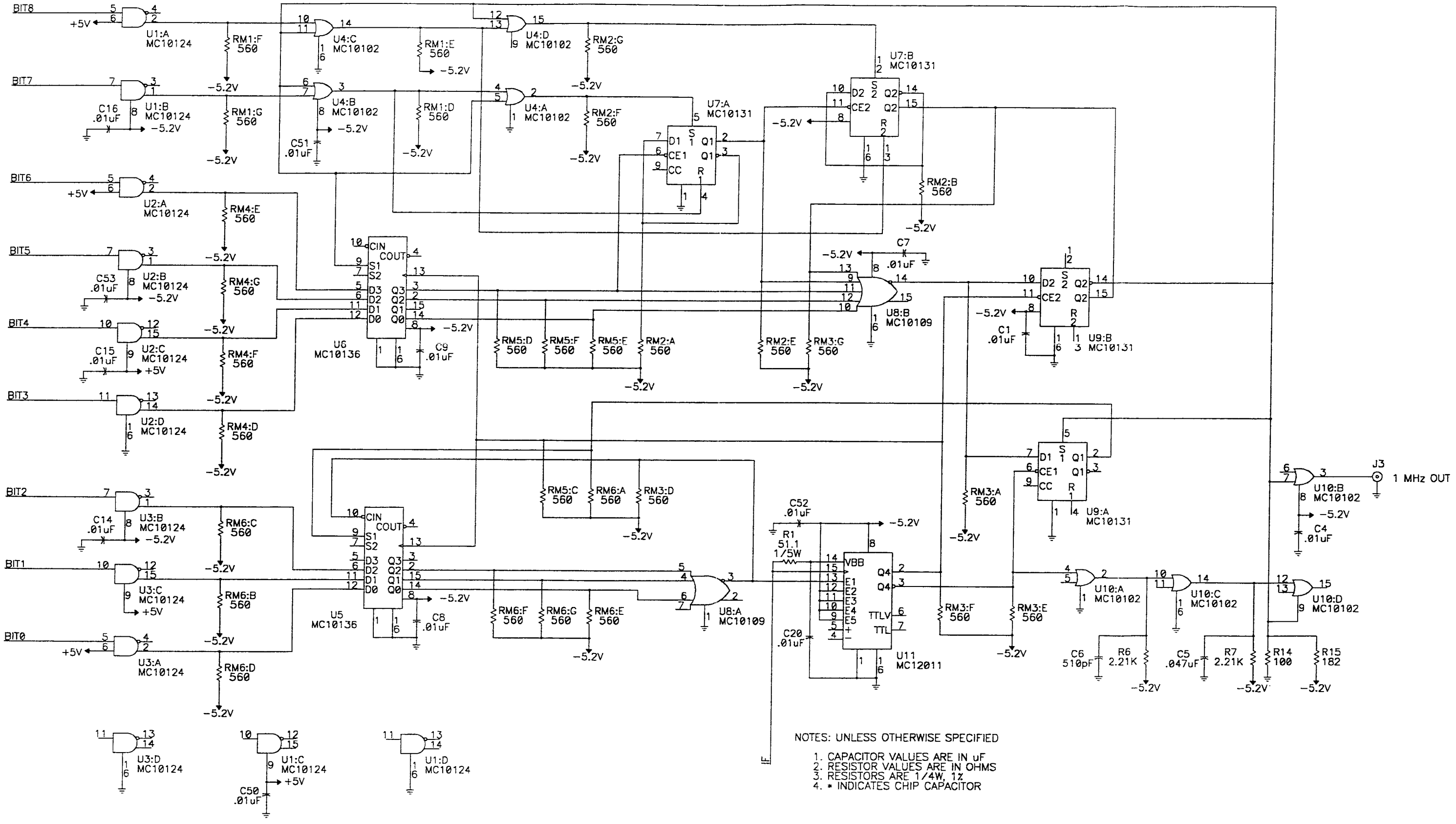
The six-bit counter (U6 and U7) continues counting down after U5 has reached zero and U11 has entered the Mod-8 phase of the division cycle. The lowest number it ever counts down from is 11, (binary 001011) whereas the highest number the three-bit counter ever counts down from is 7 (binary 111); therefore the three-bit counter always finishes first. When the six-bit counter has completed its count, gate U8-14 goes high; this line, applied to the 'D' inputs of U9, allows U9-14 to go low (this represents the falling edge of the output waveform) on the next clock transition; the output is also used to preset the six-bit counter. The three-bit counter is preset by U9-2; this transition occurs a half-cycle later than for the other counter because U9-2, unlike U9-15, is triggered by the complement of the divider circuit's clock (U11-3). The delays involved in driving the output low, presetting the counters, and triggering them to count down again result in the addition of two clock cycles to the division cycle--that is, U11 will perform two extra divisions by 8 before the next division cycle can begin. To compensate for this, U6's Q1 output is not connected to the OR gate U8-14; the six-bit counter counts down only to two, not to zero, before sending to U9 the high level that initiates the output transition and presets the counters. The duration of the output low pulse is one clock cycle, which is equal to eight I.F. cycles; because the I.F. is variable, the width of the low pulse varies (between about .02 and .08 microseconds).

EXAMPLE: When the divisor is to be 195 (this occurs when the I.F. is 195 MHz), the translators are programmed with the binary equivalent of 195 (011000011). This breaks down as 3 for the three-bit counter (binary 011), and 24 for the six-bit counter (binary 011000). For the first three clock cycles U11 divides the I.F. by 9, for a total of 3 X 9 = 27 I.F. cycles. The three-bit counter then reaches zero and programs U11 to divide by 8 for the remaining clock cycles (21, since three of the six-bit counter's 24 cycles have already been counted simultaneously with the other counter). After 21 X 8 = 168 further I.F. cycles (bringing the total so far counted to 195) the low-going pulse of the output waveform occurs, the counters are preset and the division cycles recommences. Of course, to compensate for the cycles added by delay in presetting the counters, the six-bit counter actually stopped early by 2 clock cycles (2 X 8 = 16 I.F. cycles); the high level at U8-14 occurs two clock cycles before the beginning of the next division cycle because two clock pulses are needed to initiate that division cycle. Since 195 I.F. cycles occurred during one division cycle, the circuit has divided the input frequency by 195.

The OR gate U10 and four passive components are used to shut down the output of the circuit under conditions that would interfere with normal operation of the phase lock loop. Under normal conditions, with an I.F. input in the 95-395 range, the clock frequency applied to U10-4 will be above 10 MHz. The filter components between the three gates produce a low at U10-12, and the third gate does not interfere with the circuit output frequency. If the I.F. drops substantially below the normal range, however, and the clock frequency at U10-4 falls well below 10 MHz, the filter action will not be sufficient to have the same effect; U10-9 will go to an ECL high, preventing any waveform from reaching the phase lock loop. The reason for this precaution is that the Mod 8/9 counter responds erratically to frequencies below its intended range, and could prevent the PLL circuit from recovering phase lock when the output frequency is too low. When the output waveform has been shut down, the PLL circuit reacts by "kicking" the output frequency to a higher value; this forces the I.F. to a higher frequency within the range of the divider circuit. After the I.F. has been forced higher, the "kicker" circuit again allows the output frequency to reach the PLL.

U16, 17, 18, 19 and 20 provide drive for the REFerence COUPLER and the REFerence SWITCH filters. U18 B signal is used to switch the downconverter coupler port in the 2-8 and the 8-20 modules.

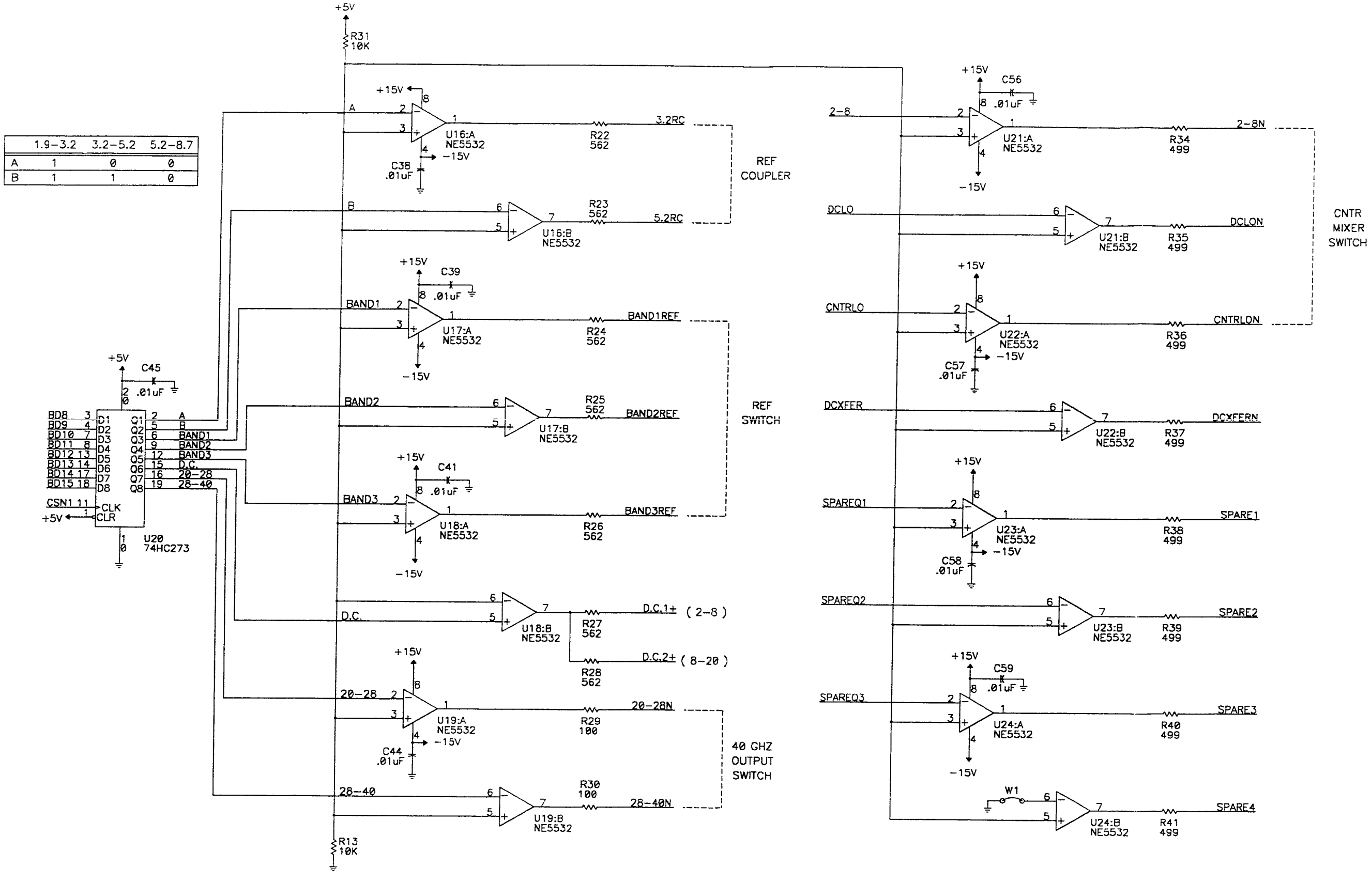
U15 is a decoder which provides decoding of chip selects. U13 and U14 are buffers required for interfacing with the computer bus.



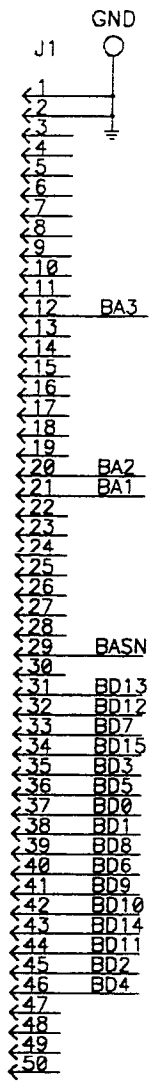
NOTES: UNLESS OTHERWISE SPECIFIED

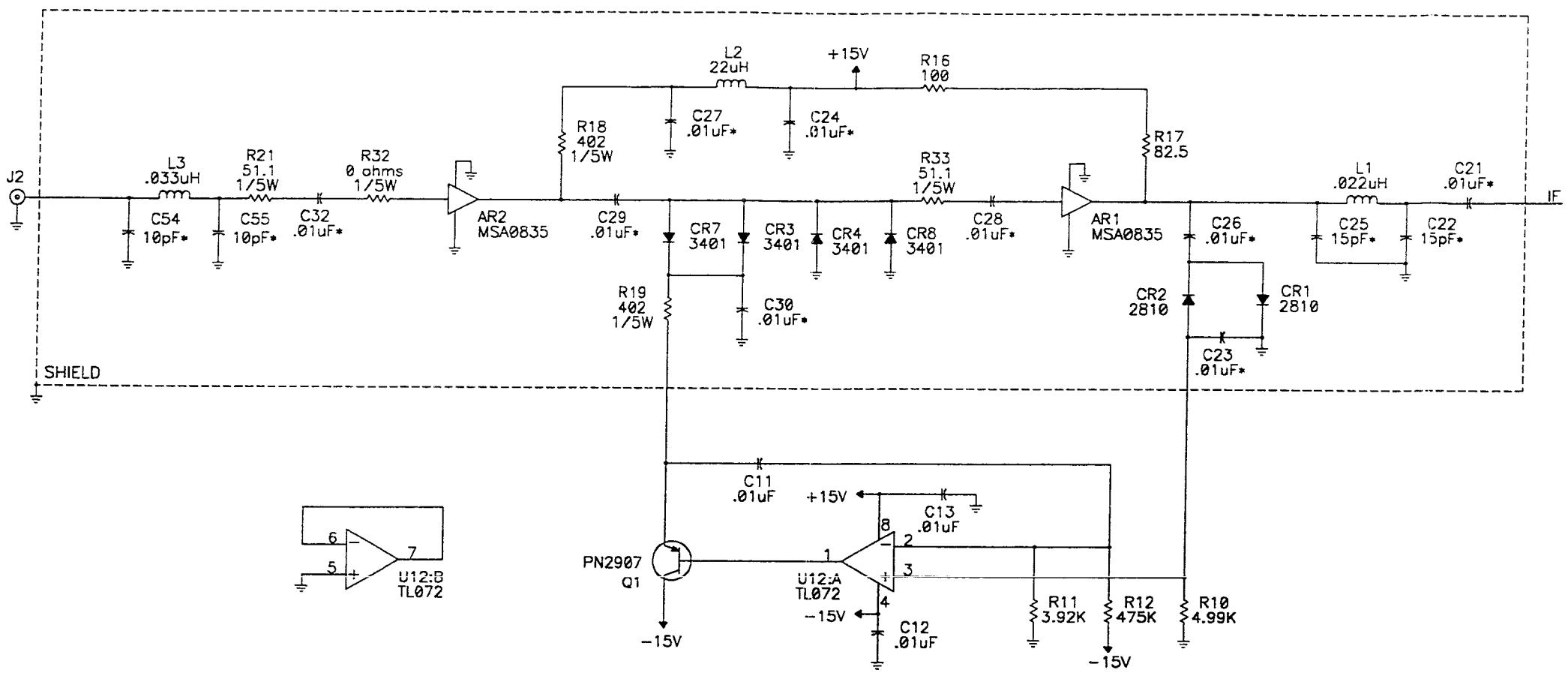
1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/4W, 1%
4. * INDICATES CHIP CAPACITOR

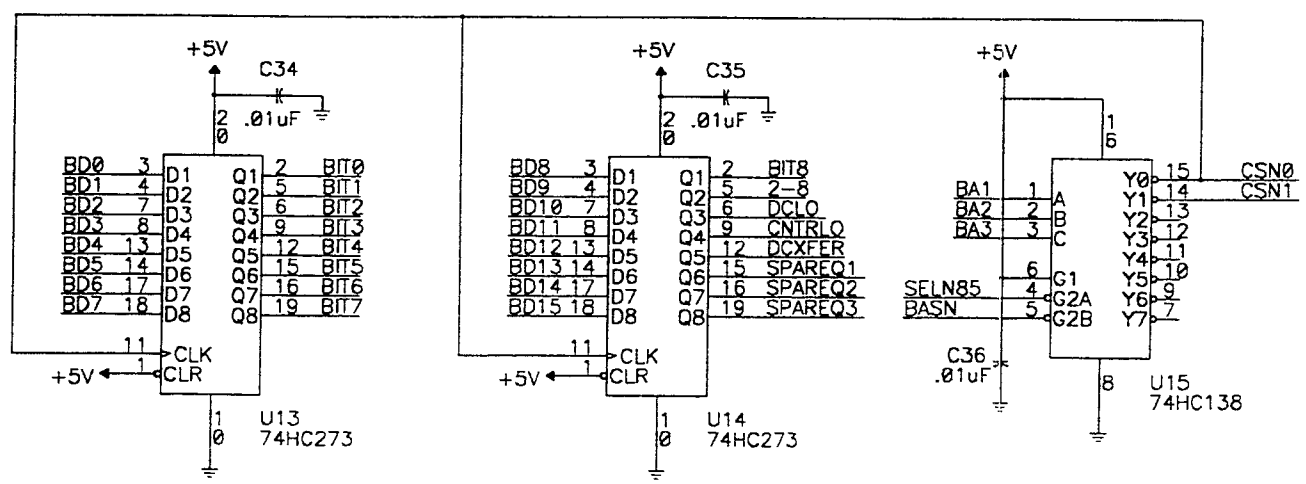
Divide By N (A17)
ASSY# 120BA07100 Rev H
Sheet 3 of 5
7-A17-3

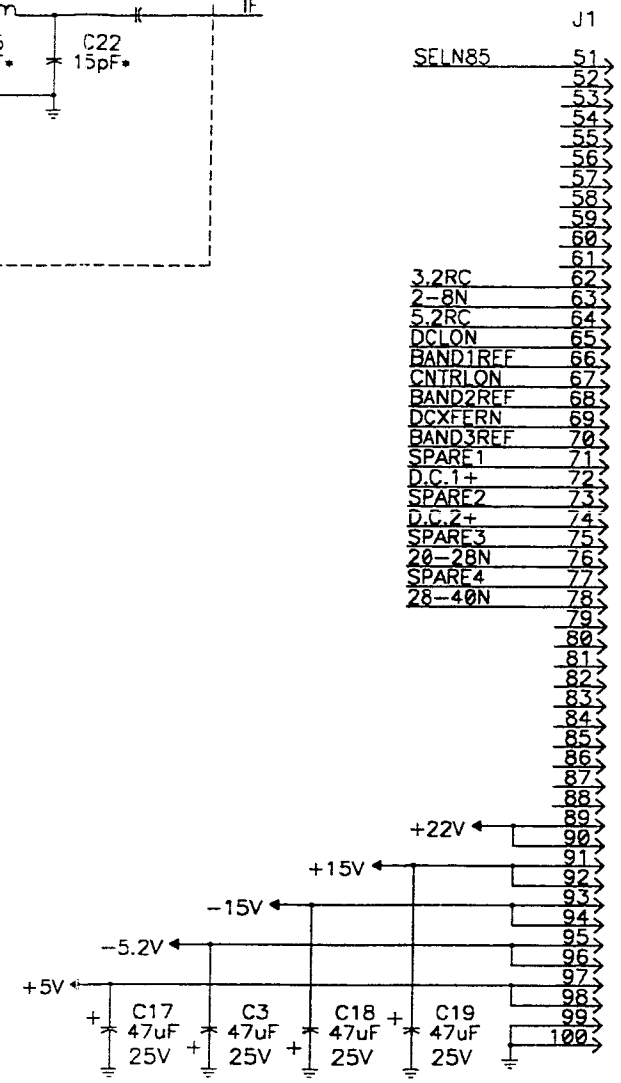


Divide By N (A17)
ASSY# 120BA07100 Rev H
Sheet 5 of 5
7-A17-5

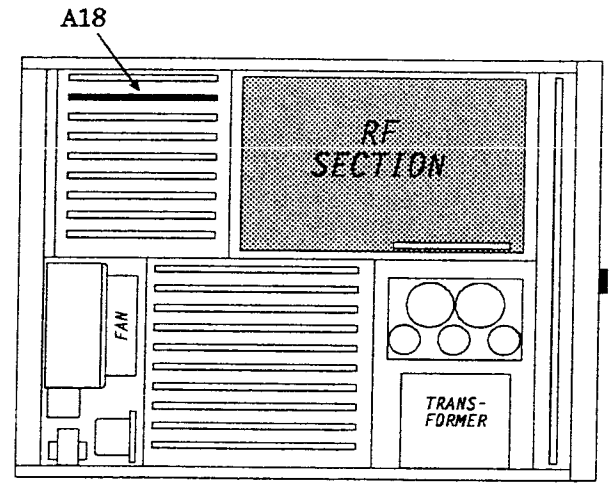




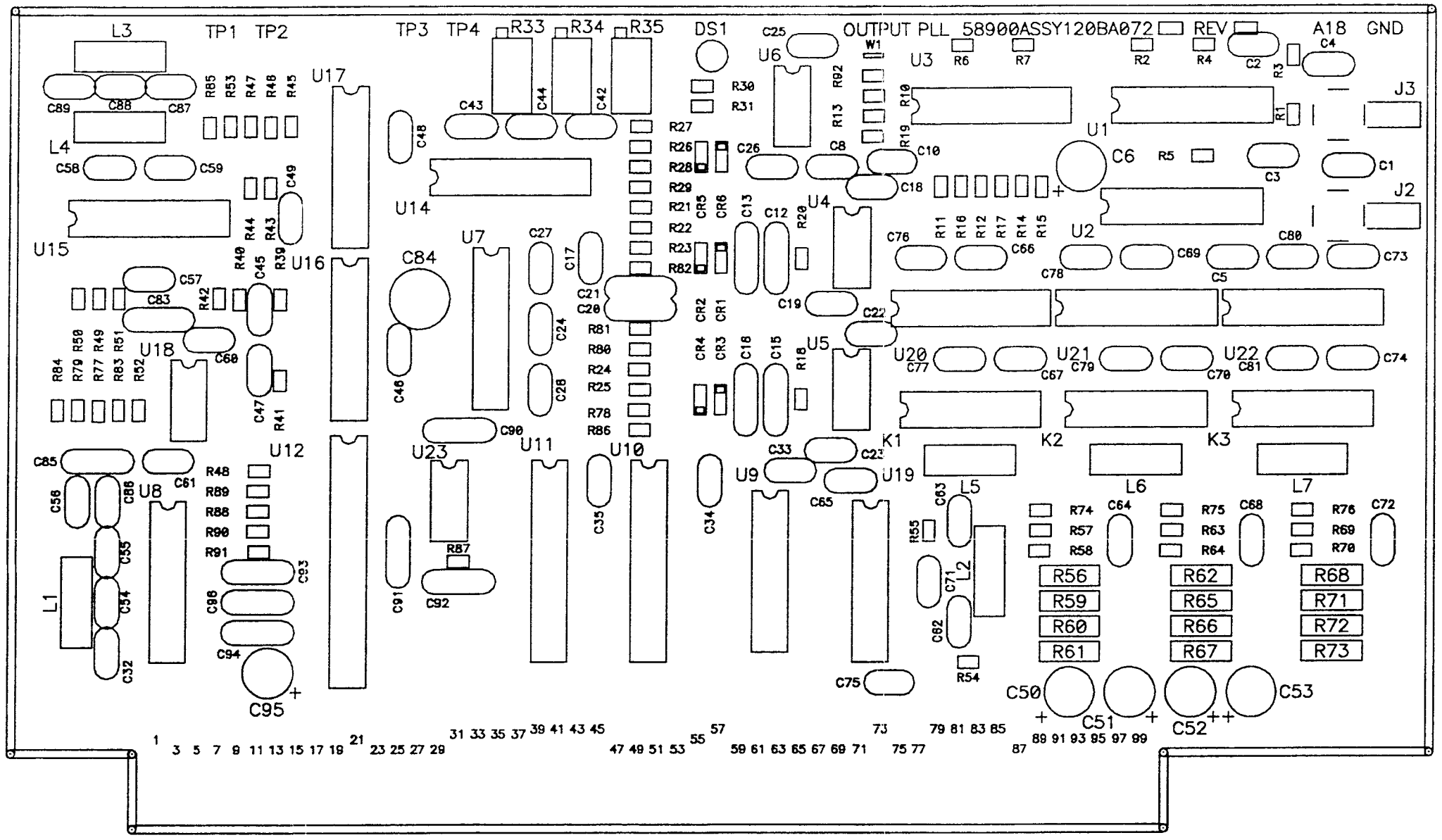




Divide By N (A17)
ASSY# 120BA07100 Rev H
Sheet 4 of 5
7-A17-4



Output PLL (A18)
DWG# 120BM07210 Rev B



OUTPUT PHASE LOCK LOOP -- PC ASSY A18

This circuit compares the output of the divide-by-N circuit (A17) to a timebase-related reference signal and fine-tunes the output YIG oscillator in order to stabilize the divide-by-N output at 1 MHz.

The 10 MHz timebase input (J3) is buffered by U1 and then applied to U3, a frequency divider with a divisor of 10. The 1 MHz output of U3 is the reference input to the phase detector U2-6. The variable input at U2-9 is the output of the divide-by-N circuit (J2), buffered by U1, which will be at 1 MHz when the loop is locked, thus giving the correct RF output frequency. If the two inputs to the phase detector are not in phase, wide pulses are produced at either U2-12 or U2-3, depending on whether the variable input is leading or lagging the reference. The loop amplifier/filter circuit U4 A and B averages these pulses in order to produce a fine-tuning signal for the output YIG oscillator. The object is to adjust the oscillator frequency in the direction that will reduce the phase difference between the inputs to the phase detector U2.

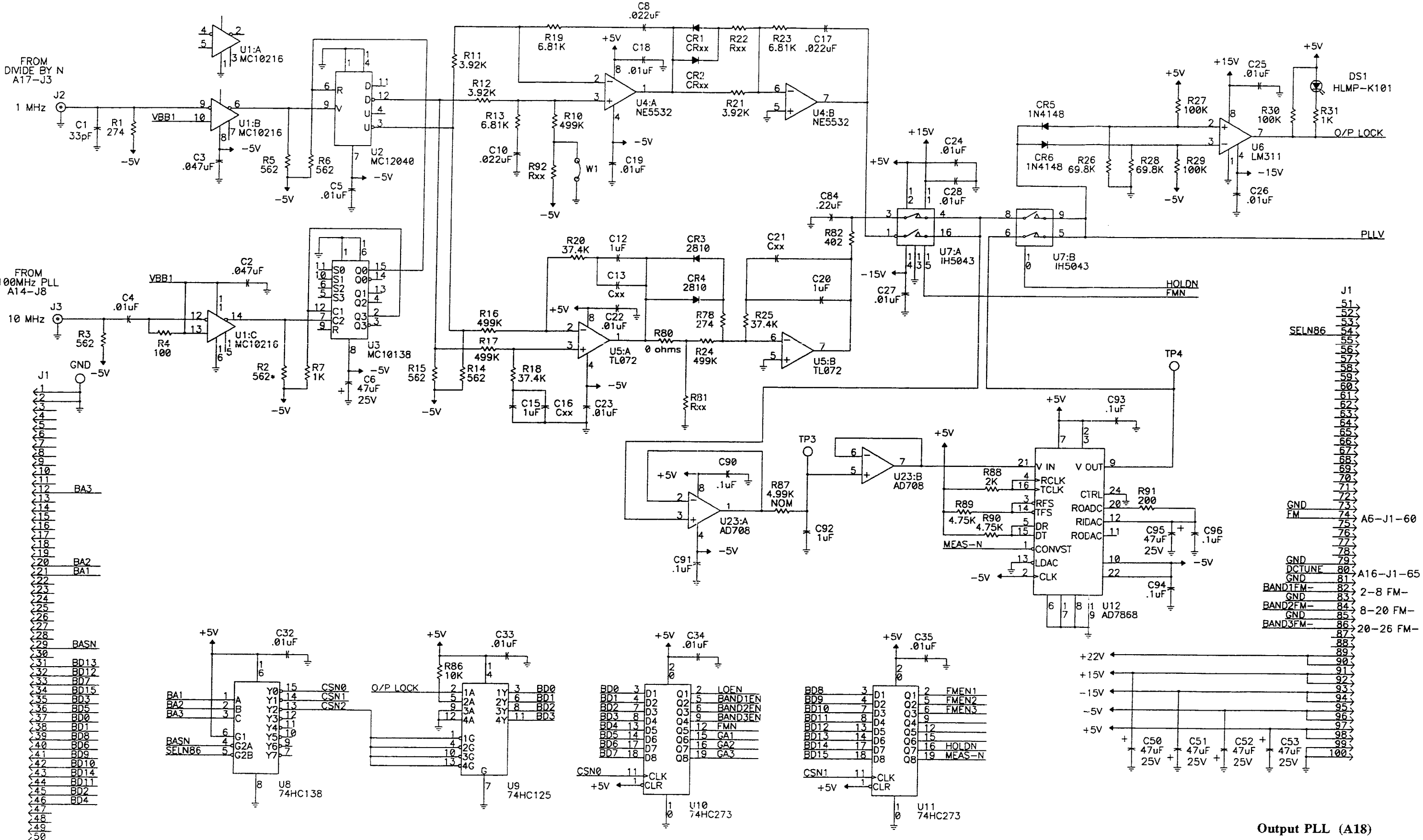
In CW mode the output of the amplifier/filter U4 A and B is applied via analog switches U7 A and B to a low pass filter (C54-56 & L1), required to filter out the 1 MHz reference frequency. The output of the filter is then applied to U18 B, an amplifier with variable AC gain used to compensate for loop gain changes due to a changing divide-by-N. R83 and R84 provide AC attenuation. The PLL voltage is buffered by U18 A before being applied to one of three summing junctions. Analog switches U19 A & B select one of 3 circuits, U20, U21, or U22, which drive the FM tuning coils of the output YIG oscillators for each frequency band.

U6 is a lock detector circuit which detects when the loop voltage goes beyond a given window, thus indicating that the loop is unlocked. This circuit pulls the output lock signal low, causing the lock LED DS1 to light. When the loop voltage is within the window the loop is locked, the OUTPUTLOCK logic line is high and the lock LED on the PC board is dark.

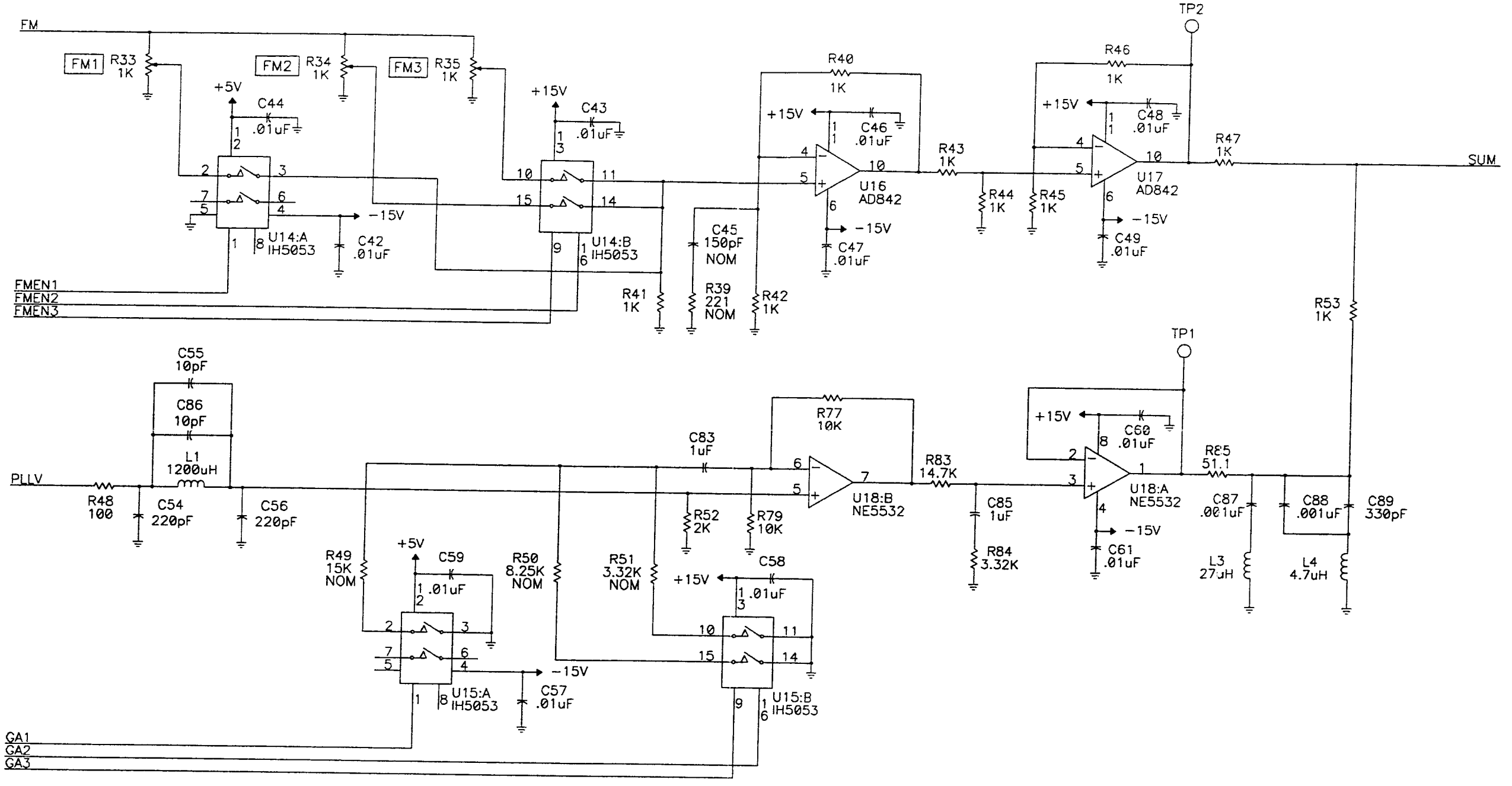
When the FM mode is enabled an alternative loop amplifier/filter is required. In this case U5 A and B filter the output pulses of the phase detector. The outputs of both amplifier/filter circuits, U5 and U4, are applied to U7, an analog switch. When the FM mode is selected and the switch U7 A enables the U5 amplifier/filter. Additionally, during FM mode the modulating signal is summed in with the loop voltage at one of the 3 FM drive circuits U20, 21, 22. The modulating signal sensitivity is adjusted via R33, R34, or R35, depending on which frequency band is active. The appropriate sensitivity is selected via switch U14 A & B and the modulating signal is then amplified by U16 and U17. U19 A switches the PLL voltage from the fixed LO PLL PCA to the 2-8 GHz oscillator when required for downconversion of frequencies below 2 GHz.

U12 operates as a sample and hold circuit during Analog Sweep operation by holding the PLL loop voltage, thereby setting the START frequency, when the analog switch U7-B receives the HOLDN low logic signal.

U8 provides an interface between the computer and the PCA by decoding the chip select lines. U9 buffers the output logic from the PCA so that it can be read by the computer. U10 and 11 are latches for logic input from the computer bus.



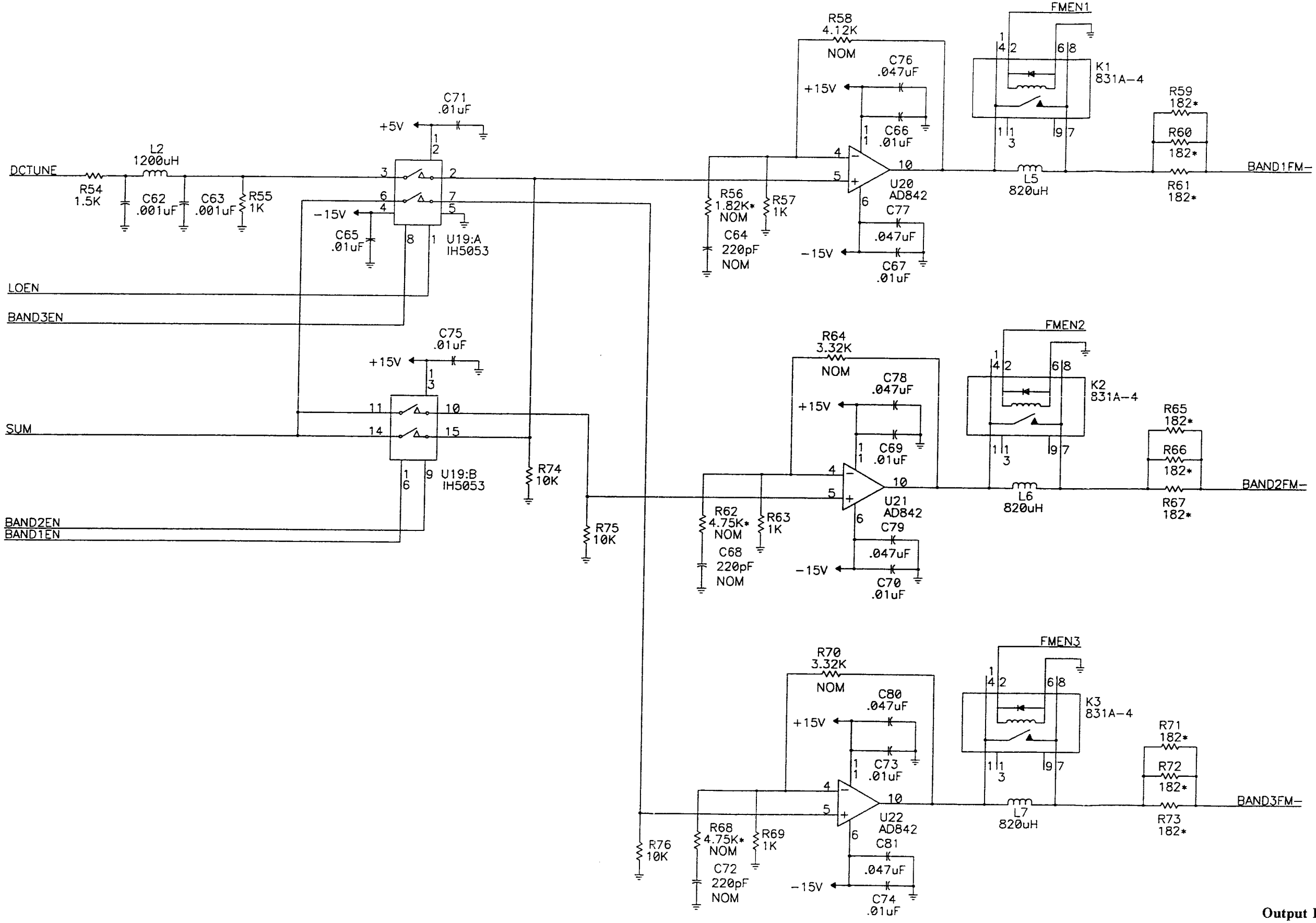
Output PLL (A18)
DWG# 120BM07210 Rev B
Sheet 3 of 5
7-A18-3



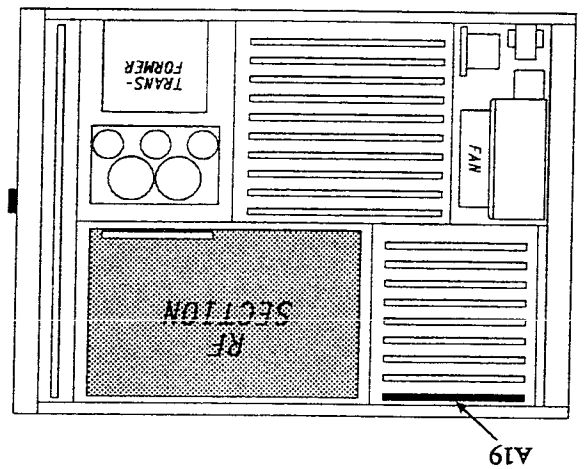
NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN uF.
2. RESISTOR VALUES ARE IN OHMS.
3. RESISTORS ARE 1/5W, 1%
4. * INDICATES 1/4W, 1% RESISTORS.

Output PLL (A18)
DWG# 120BM07210 Rev B
Sheet 4 of 5
7-A18-4



Output PLL (A18)
DWG# 120BM07210 Rev B
Sheet 5 of 5
7-A18-5

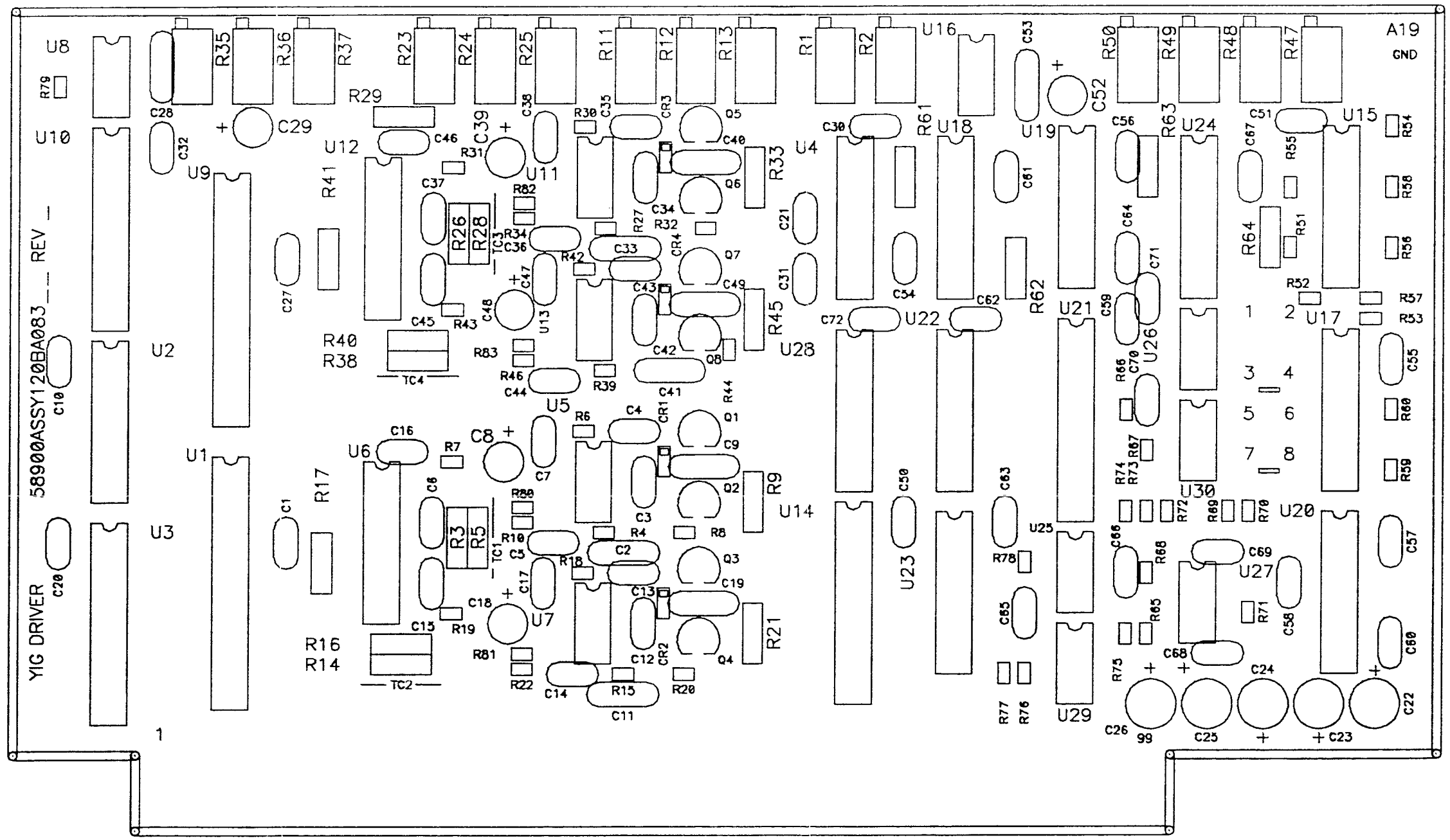


VTG Driver (A19)

ASSY# 120BA08300 Rev J

Sheet 1 of 5

7-A19-1



YIG DRIVER – PC ASSY A19

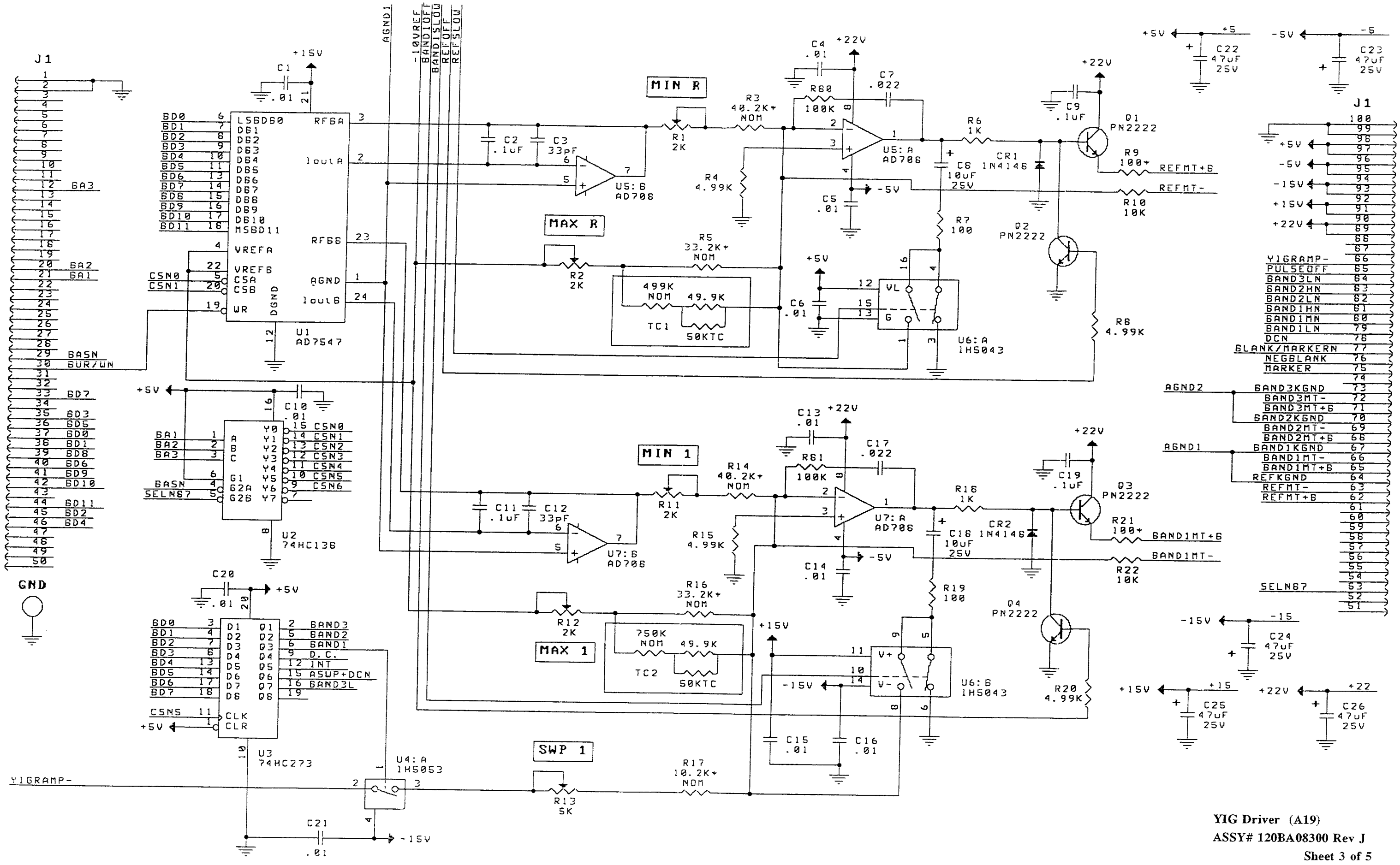
The YIG Driver PCA consists of 4 YIG driver circuits, one for each of the frequency bands (2-8, 8-20, 20-26GHz and the Reference oscillator). In addition, this board holds the circuitry which generates the logic for different frequency bands, and for switching filters in RF modules. It also generates logic used during sweep.

The YIG driver circuit for BAND1 consists of DAC U1 section B whose output is converted to voltage by U7 B. MIN 1 pot (R11) is used for adjusting the voltage to the YIG when at the minimum frequency in band 1. The reference voltage is also summed in at U7-2 thru MAX 1 pot (R12) which is used to adjust the voltage provided to the YIG when at the maximum frequency in band 1. At the output of U7 A there is a filter which can be switched in by U6 B when the Unit is in CW or 'SLOW' mode, ie, when the Unit is not sweeping or changing frequency. This filter is disabled, when the unit is sweeping or changing frequency, allowing the YIG voltage to change rapidly. This switched filter is known as the 'Fast/Slow' circuitry. When analog sweep is activated U4 A is switched allowing a ramp voltage to be summed into the amplifier U7 to sweep the YIG thru the specified band. Q4 is required to turn off the tuning voltage to the YIG when the band is not selected. Q3 provides the drive for the Main tune coil of the YIG.

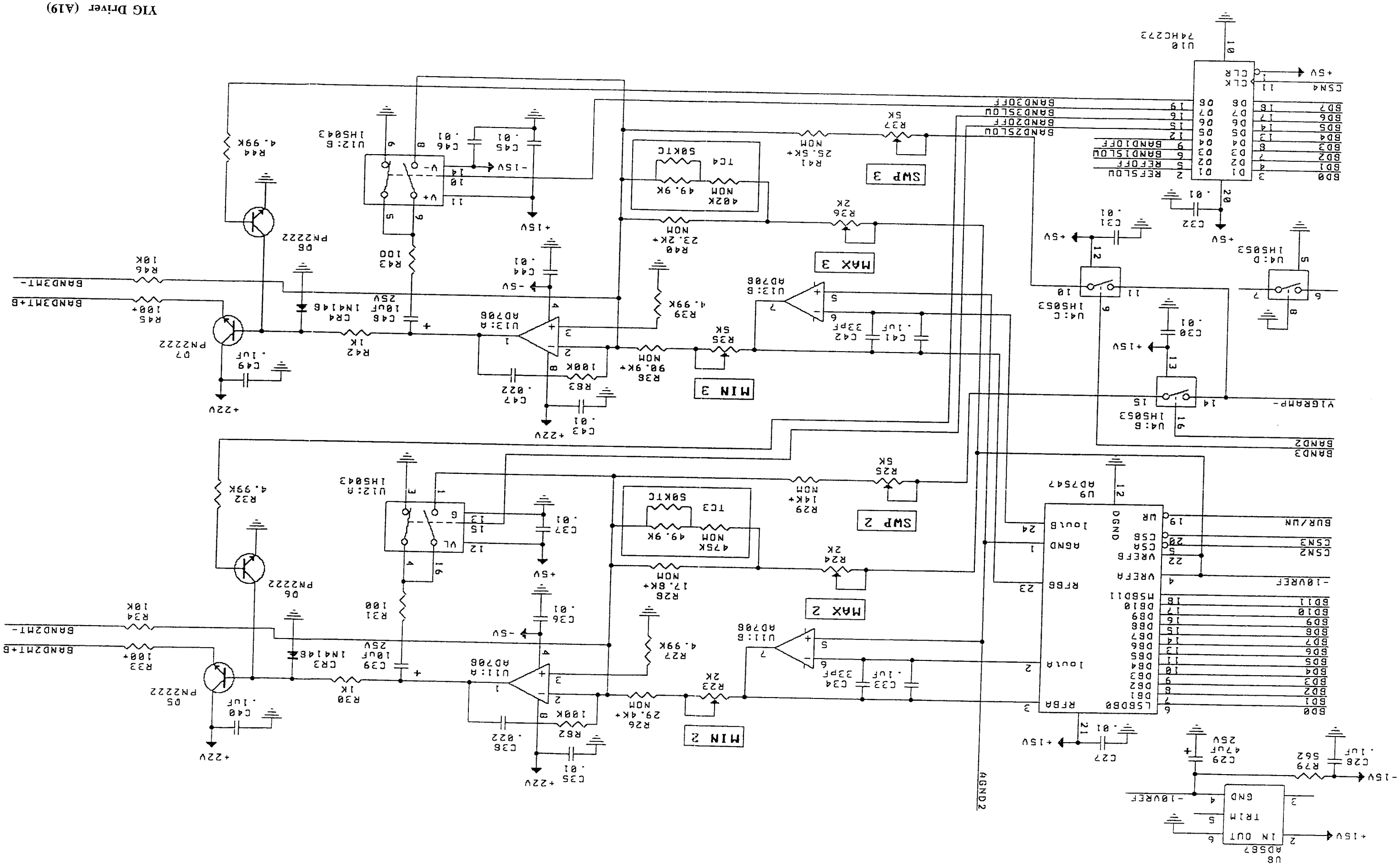
This circuit is repeated for each of the bands. The only difference is that in the reference band there is not a ramp voltage summed in during analog sweep.

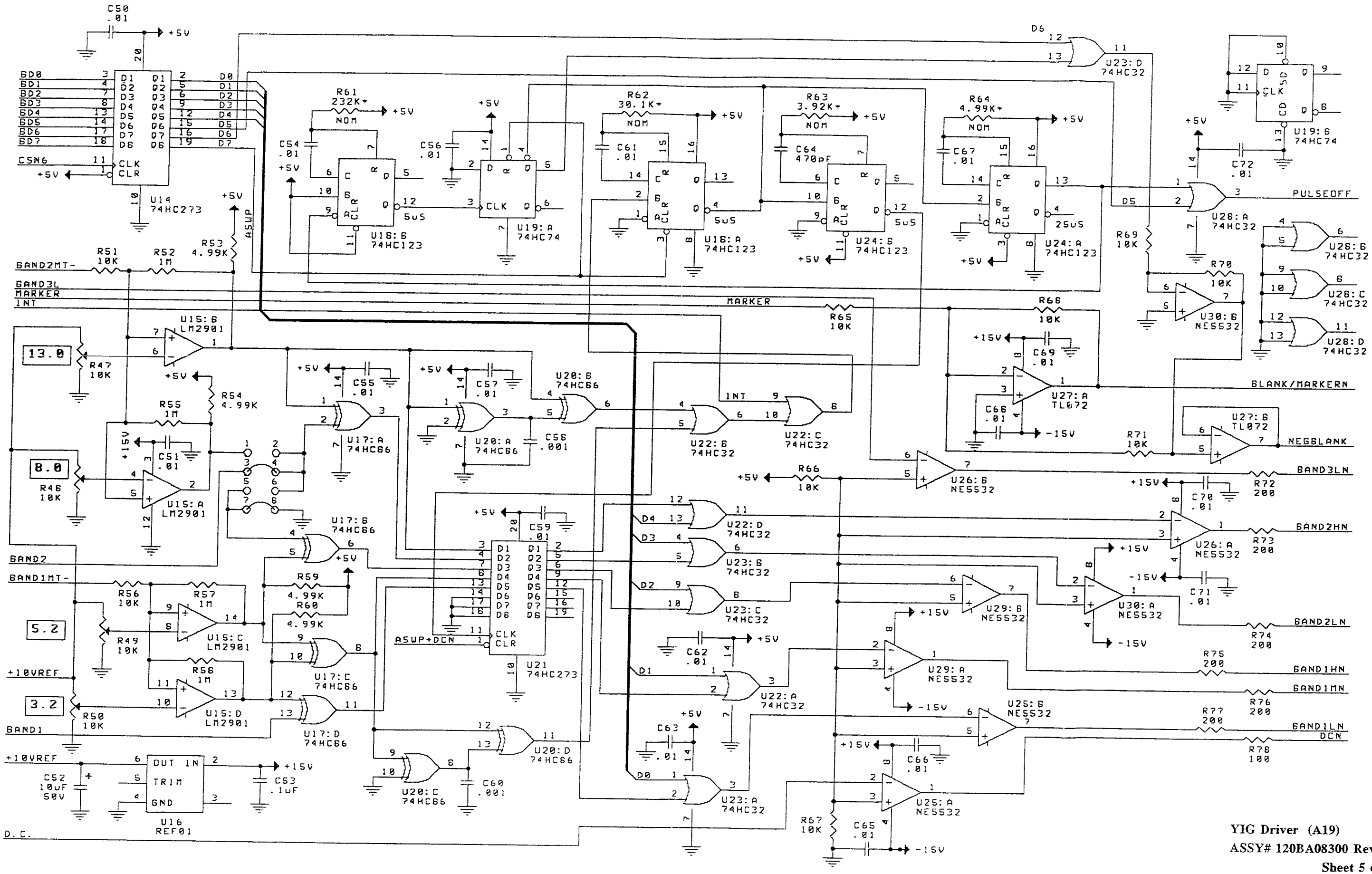
Filter switching logic and sweep logic signals are also generated on A19. When the unit is not in analog sweep U21 is cleared thereby enabling U22 and U23 to propagate the logic latched by U14 from the computer bus. These outputs drive U25 and U26 which drive the filter switches for the output switch module. When the unit is in analog sweep, the computer cannot provide the logic signals at the appropriate times therefore another method is used to detect when to switch the filters. For example, in band 1 this method involves sampling the main tuning voltage and using a comparator U15 C to detect when the main tune voltage reaches a voltage set by the 5.2 pot (R49). This 5.2 reference voltage can be adjusted to insure that the comparator output switches when the frequency is at 5.2 GHz. The output then propagates thru to U21 which is enabled during analog sweep. The remaining logic along with flip flops U18, U19 and U24 work in conjunction to supply the remaining filter logic and blanking signals required during analog sweep.

Decoder U2 decodes the chip select lines for circuits on this PC board. U3, U10 and U14 are required for computer bus interface.

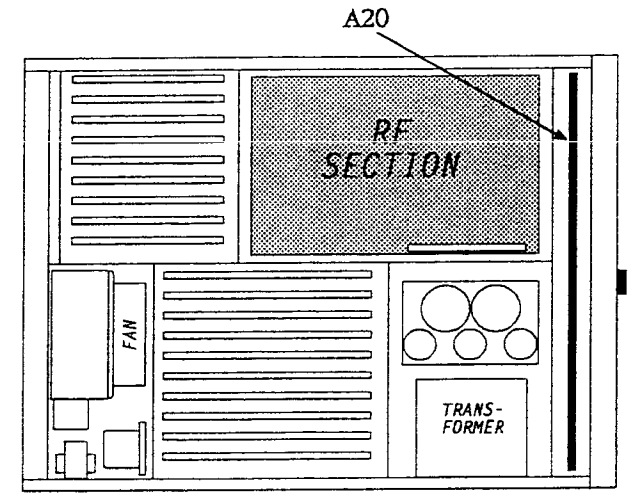


YIG Driver (A19)
ASSY# 120BA08300 Rev J
Sheet 3 of 5
7-A19-3

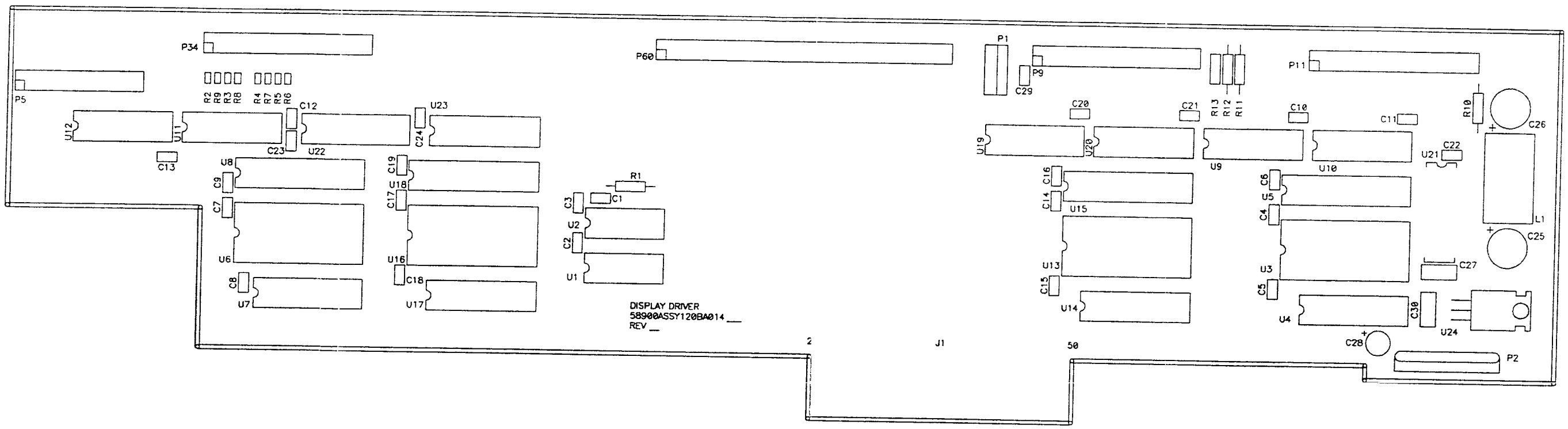

U10 74HC273
CSN4
SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7
REFSLOU REFOFF BAND1SLOU BAND1OFF BAND2SLOU BAND2OFF BAND3SLOU BAND3OFF
C32 .01
C31 .01
U4:D 1HS053
U4:C 1HS053
U4:B 1HS053
C30 .01
+15V
VIGRAMP-
BAND3
BAND2
U9 AD7547
BUR/WN
CSN3
CSN2
-10VREF
SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7 SD8 SD9 SD10 SD11
C27 .01
C29 47UF 25V
R79 562
C28 .1UF
-15V
U8 AD587
SWP 3
MAX 3
MIN 3
R41 25.5K* NOM
R37 5K
TC4 50KTC
R40 23.2K* NOM
R36 2K
R39 4.99K
R35 5K
R38 90.9K* NOM
C41 .1UF
C42 33PF
U13:B AD708
U12:B 1HS043
C46 .01
C45 .01
R44 4.99K
D8 PN2222
R43 100
C48 10UF 25V
CR4 1N4148
R46 10K
R45 100*
BAND3MT-
BAND3MT+B
Q7 PN2222
C49 .1UF
R42 1K
C44 .01
C43 .01
U13:A AD708
C47 .022
R53 100K
+22V
SWP 2
MAX 2
MIN 2
R29 14K* NOM
TC3 50KTC
R25 5K
R24 2K
R28 17.8K* NOM
R27 4.99K
R26 29.4K* NOM
R23 2K
C34 33PF
C33 .1UF
U11:B AD708
U12:A 1HS043
C37 .01
C36 .01
R32 4.99K
D6 PN2222
R31 100
C39 10UF 25V
CR3 1N4148
R34 10K
R33 100*
BAND2MT-
BAND2MT+B
Q5 PN2222
C40 .1UF
R30 1K
C38 .022
R52 100K
C35 .01
AGND2



YIG Driver (A19)
ASSY# 120BA08300 Rev J
Sheet 5 of 5
7-A19-5



Display Driver (A20)
DWG# 120BM01401 Rev D
Sheet 1 of 4
7-A20-1



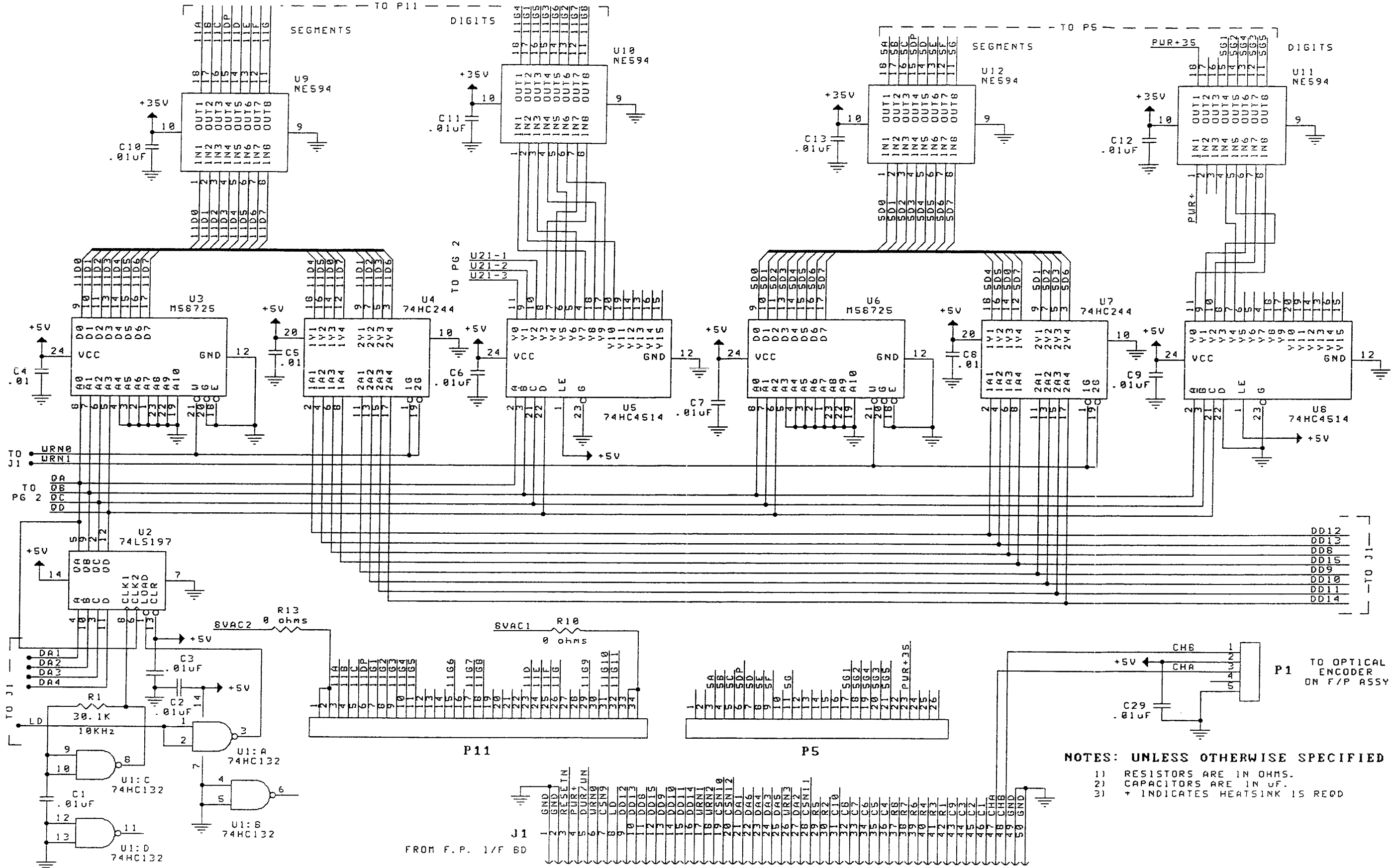
DISPLAY DRIVER -- PC ASSY A20

This board holds the necessary circuitry to drive the fluorescent displays and the LEDs on the front panel.

U2 is a counter which is clocked by U1 thereby cycling thru the addresses corresponding to each display digit and its segments. When the computer updates the display or when a setting has been changed, the LD line is activated, and the counter U2 stops counting and outputs the address which is on its A-D inputs, to QA-QD outputs thus addressing the decoders and RAMS when the appropriate chips are selected by the read/write lines. At this time data is available at the input of the latch U4 and can be loaded into the RAM U3. When the data has been updated for all addresses, the LD line becomes inactive and the counter U2 again cycles thru the addresses, selecting data for specific segments to be driven via U9. At the same time decoder U5 decodes the addresses to select each individual digit via U10. This scheme is used to drive all 3 fluorescent displays.

A similar scheme is used for lighting the LEDs on the front panel, the only difference is that they are addressed by rows and columns via U22 and U23 respectively.

U24 regulates +9 V to +5 volts required for the HP alpha numeric displays on the A106 PCA.



NOTES: UNLESS OTHERWISE SPECIFIED

1) RESISTORS ARE IN OHMS.
2) CAPACITORS ARE IN uF.
3) + INDICATES HEATSINK IS REQD

Display Driver (A20)
DWG# 120BM01401 Rev D
Sheet 3 of 4
7-A20-3

P9

8VAC2

SEGMENTS 9A 9B 9C 9D 9E 9F 9G 9DP

DIGITS 9G1 9G2 9G3 9G4 9G5 9G6 9G7 9G8 9G9

9AC — R11 15 — 8VAC1

SAC — R12 56.2 — 8VAC1

U19 NE594 — +35V — C20 .01uF — 9D0 9D1 9D2 9D3 9D4 9D5 9D6 9D7

U20 NE594 — +35V — C21 .01uF — 9G1 9G2 9G3 9G4 9G5 9G6 9G7 9G8

TO P11 — 11G11 11G10 11G9

U21 NE594 — +35V — C22 .01uF — 9G9

FROM PG 1 — U21-1 U21-2 U21-3

TO P60

P34 — TO PUSHBUTTON BD.

RLN0 RLN1 RLN6 RLN7 — CG CL0 CL1 CL6 CL5 CL4 CL3 CL2 — R5 R2 R3 R8

R2 RLN0 — R3 RLN1 — R4 RLN2 — R5 RLN3 — R6 RLN4 — R7 RLN5 — R8 RLN6 — R9 RLN7

R2 - R9 ARE 0 OHM JUMPERS

U22 74HC244 — +5V — C23 .01uF — MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7

U23 74HC244 — +5V — C24 .01uF — CL7 CL5 CL3 CL2 CL0 CL1 CL4 CL6

U13 M58725 — +5V — C14 .01 — D0 D1 D2 D3 D4 D5 D6 D7 — A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 W G E — VCC GND

U14 74HC244 — +5V — C15 .01 — C16 .01uF

U15 74HC4514 — +5V — C17 .01uF — A B C D LE G

U16 M58725 — +5V — C18 .01

U17 74HC244 — +5V — C19 .01uF

U18 74HC4514 — +5V

TO J1 — WRN2 WRN3

FROM PG 1 — DA DB DC DD — DD12 DD13 DD8 DD15 DD9 DD10 DD11 DD14

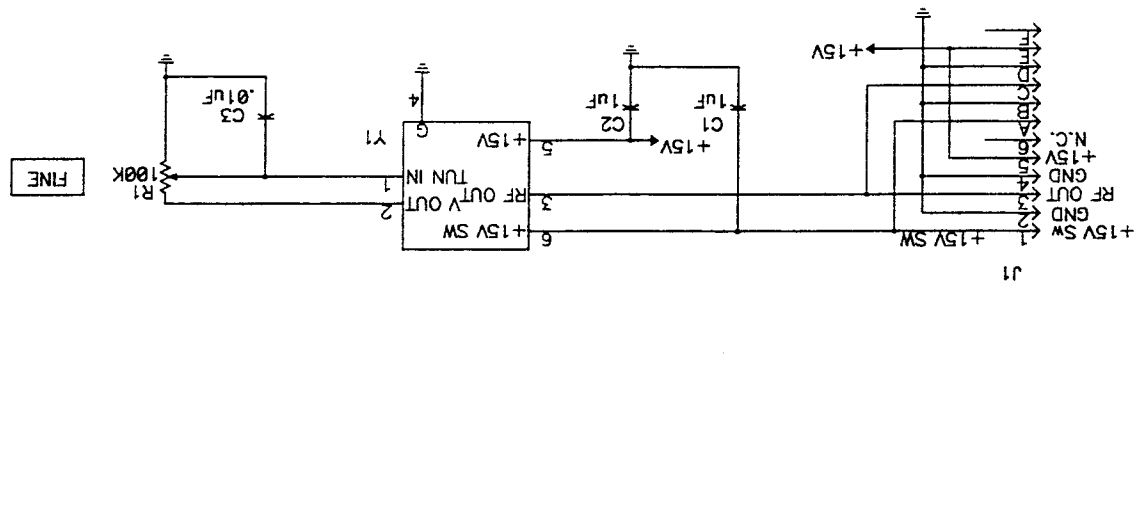
P2 — +5V — +35V — C27 1uF — C28 47uF — +5 +35 GND GNDX +9C 8VAC1 8VAC2

GNDX +9C +5C — U24 MC7805CT — +5V GND Vin — C30 1uF — L1 1mH — C25 470uF 16V — C26 470uF 16V

P60 — TO DATA ENTRY BD.

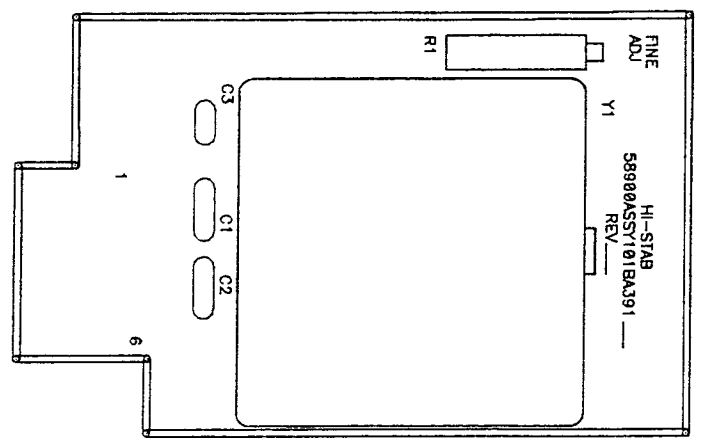
CL0 CL2 CL1 CL3 CL4 CL5 CL6 CL7 RLN4 RLN3 RESETN RLN5 DUR/WN RLN2 CSN9 DD12 DD13 DD8 DD15 DD9 DD10 DD11 DD14 GNDX GNDX CSN10 CSN12 DA1 DA6 DA4 DA3 DA5 DA2 CSN11 +5C +5C C6 C7 C6 C5 C4 R7 R6 R4 R3 R1 C9 C3 C2 C1

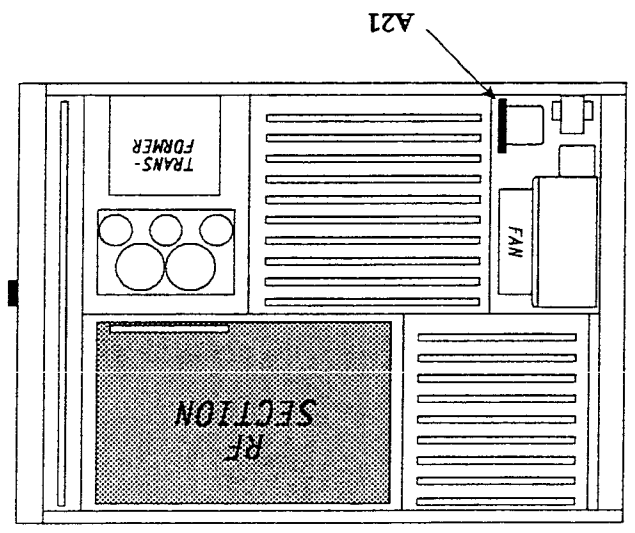
Display Driver (A20)
DWG# 120BM01401 Rev D
Sheet 4 of 4
7-A20-4



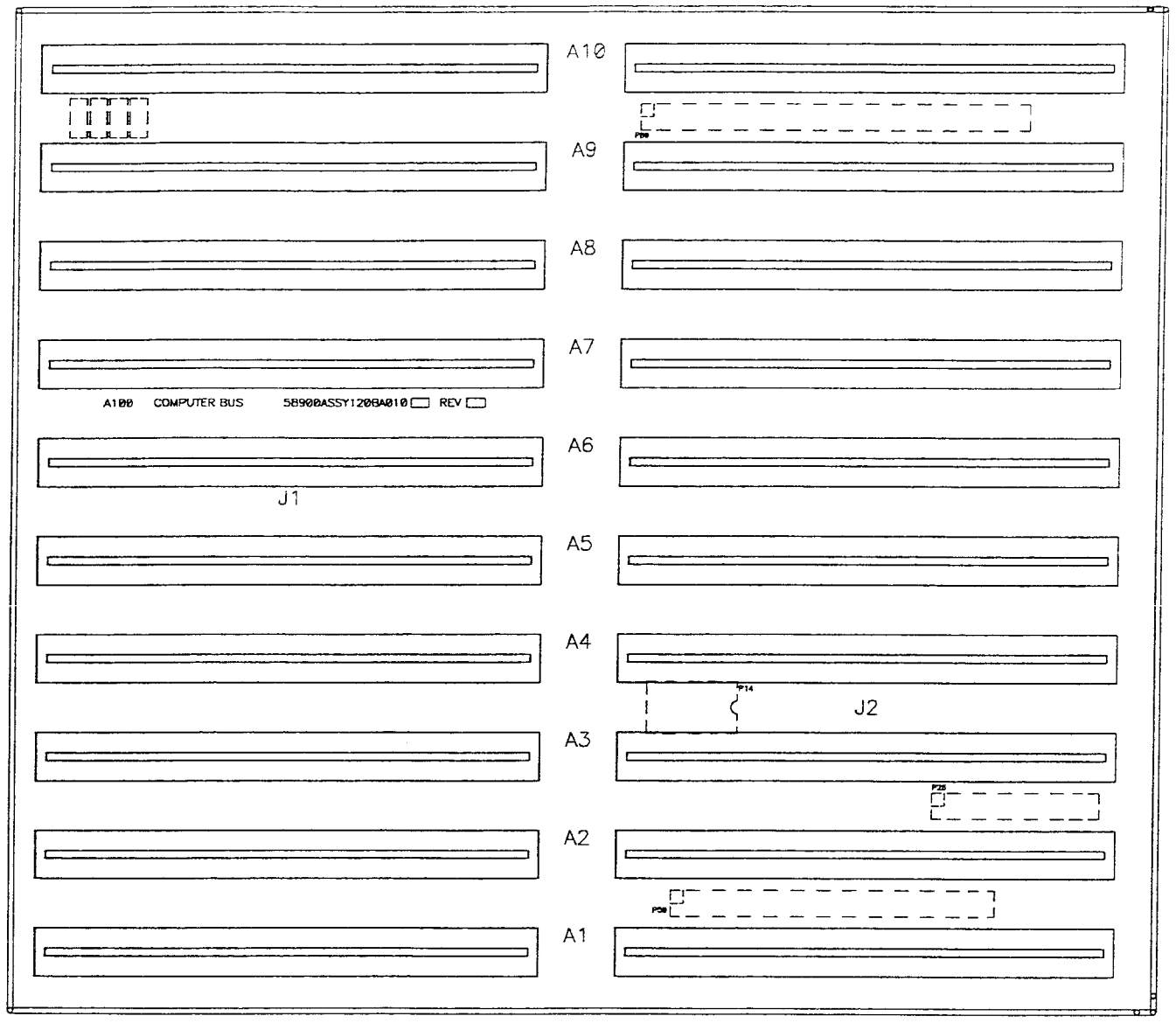
NOTES: UNLESS OTHERWISE SPECIFIED

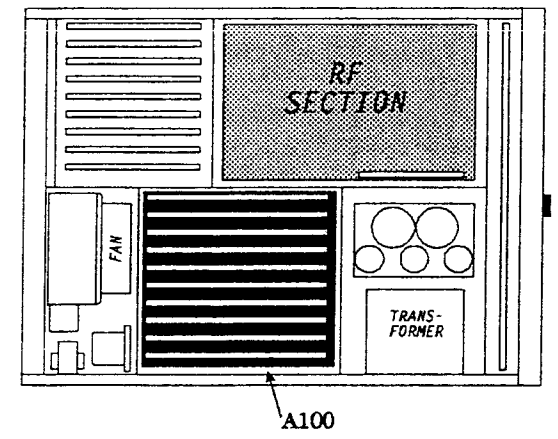
1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/5W,1%



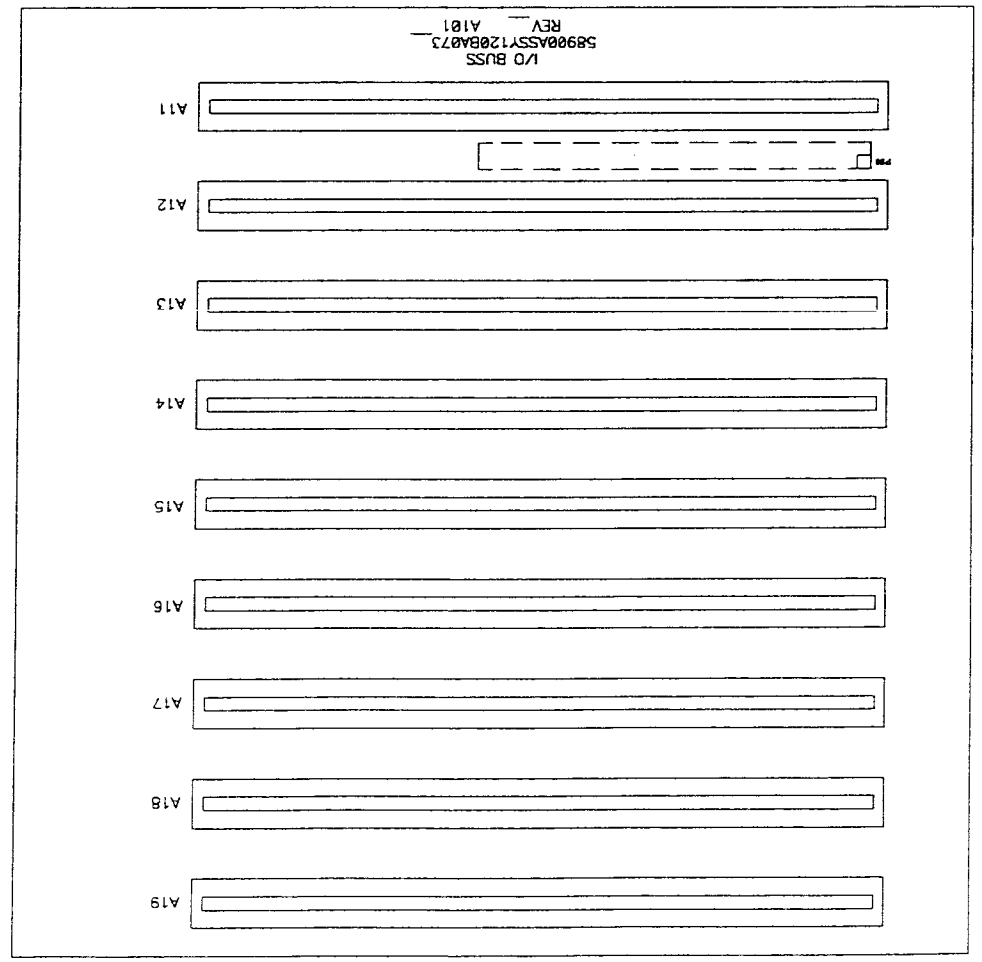


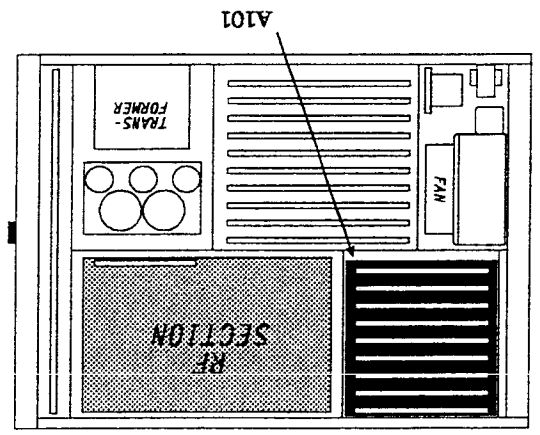
High Stability Osc (A21)
DWG# 101BM39101 Rev B
Sheet 1 of 1
7-A21-1





Computer Bus (A100)
ASSY# 120BA01000 Rev E
Sheet 1 of 1
7-A100-1



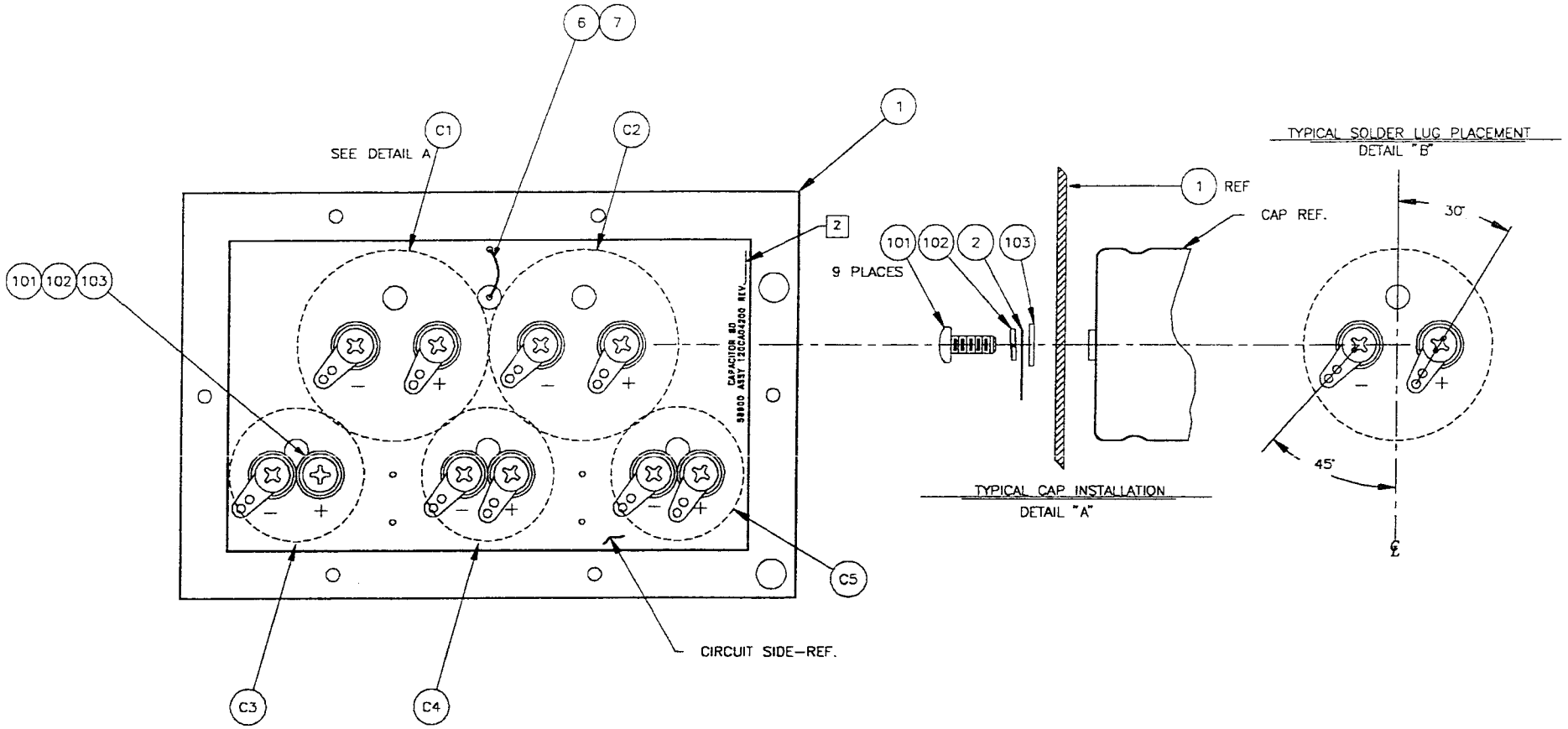


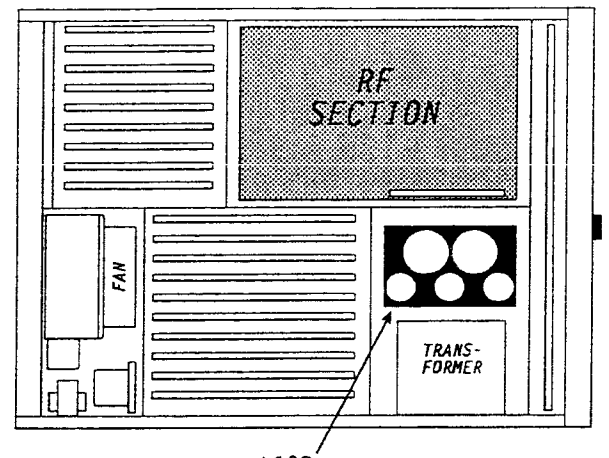
I/O Bus (A101)

DWG# 120BM07300 Rev F

Sheet 1 of 1

7-A101-1

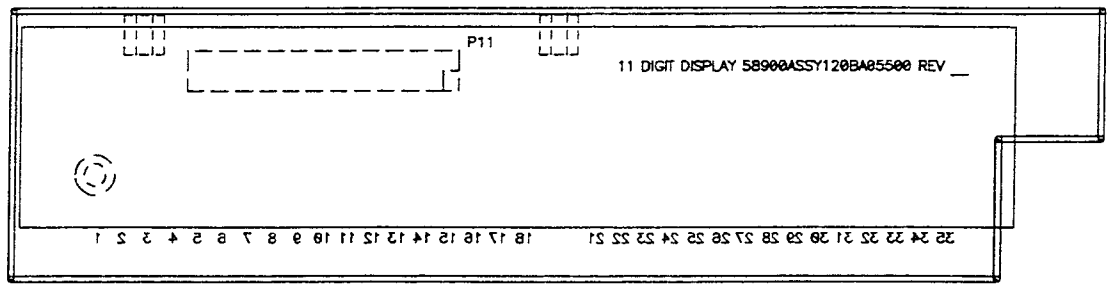


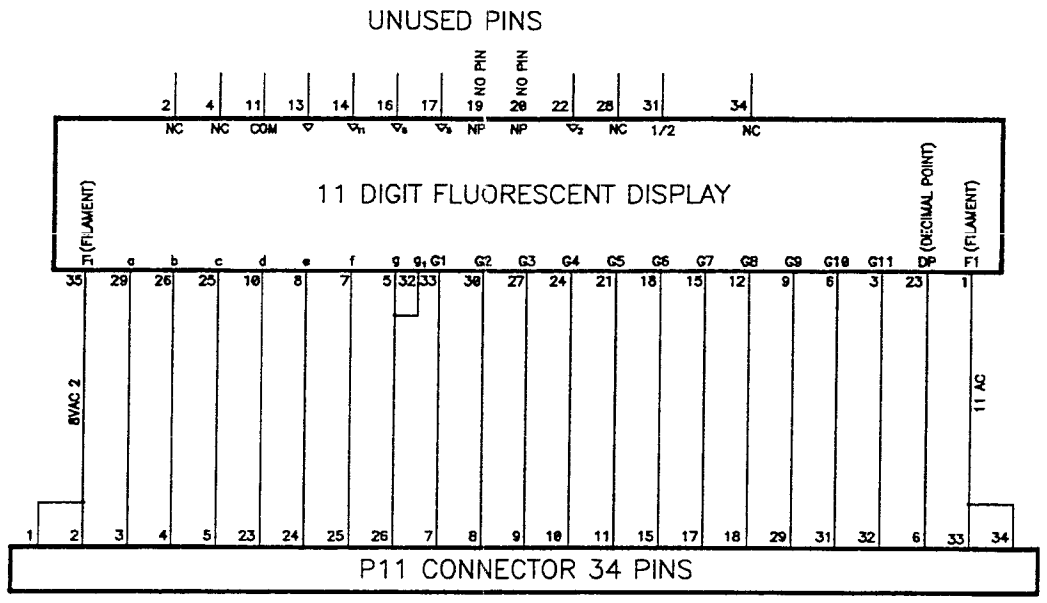


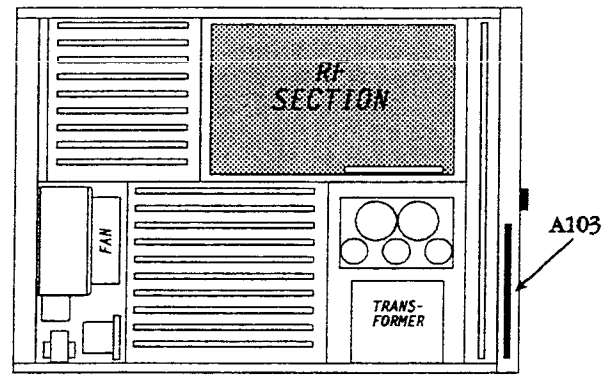
NOTES

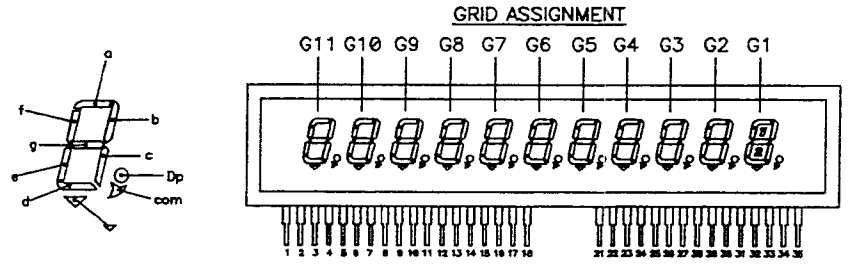
1. CAPACITORS TO BE INSTALLED FARSIDE.
2. LABEL PER DWG REV.
3. SEE SEPARATE PARTS LIST 120CA04200

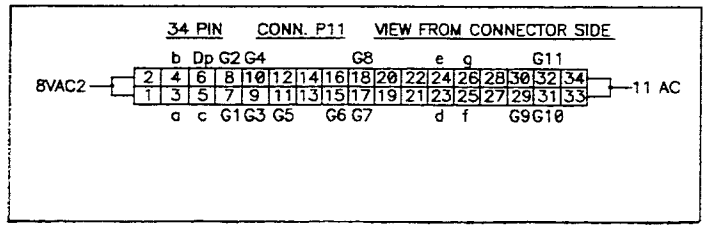
Capacitor (A102)
DWG# 120BM04200 Rev B
Sheet 1 of 1
7-A102-1



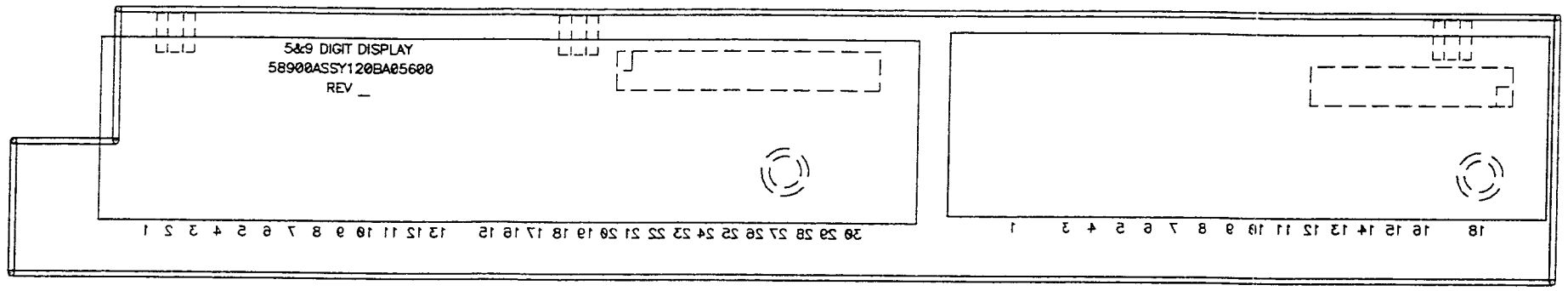




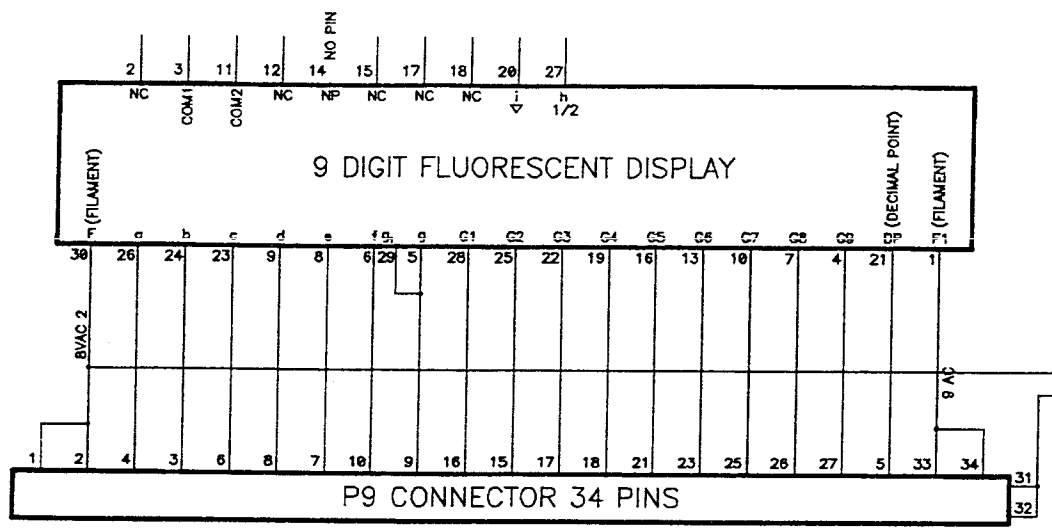


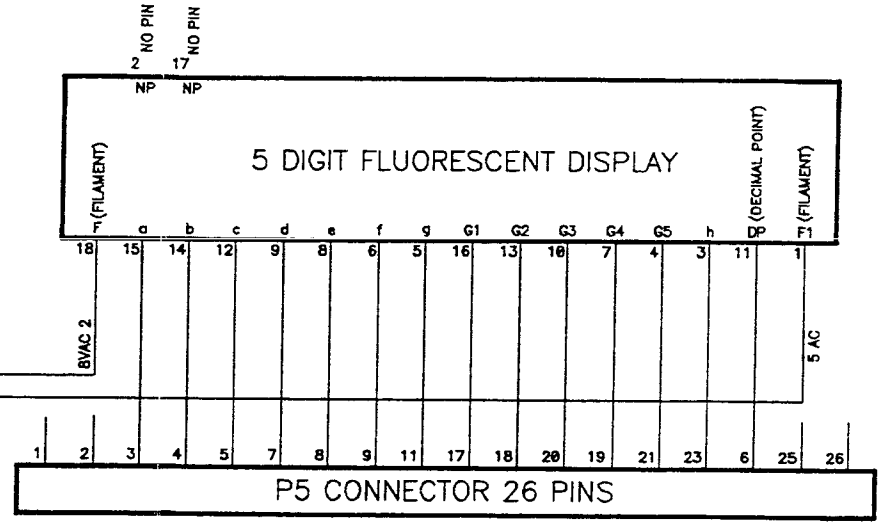


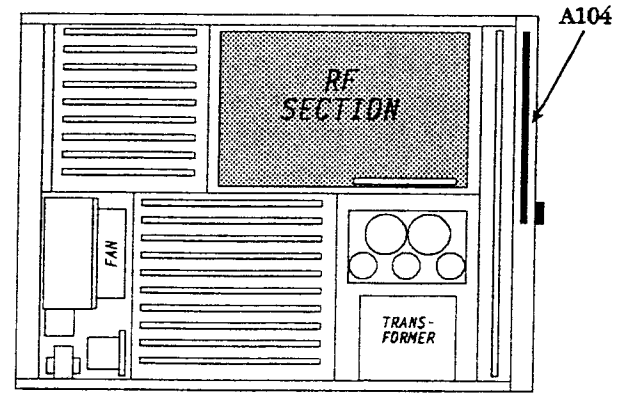
11 Digit Display (A103)
DWG# 120BM05500 Rev C
Sheet 1 of 1
7-A103-1



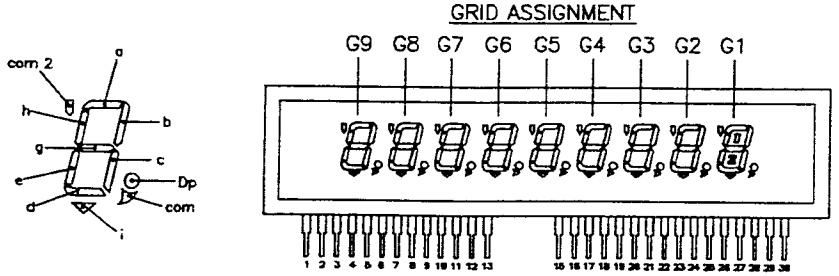
UNUSED PINS



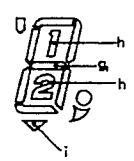




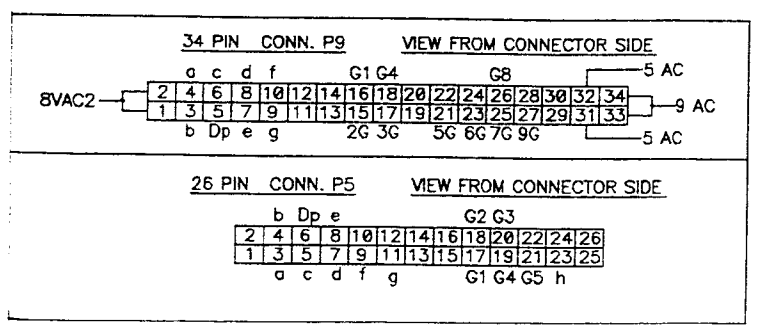
GRID ASSIGNMENT



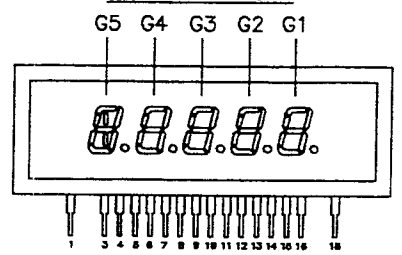
DIG 1 thru 9

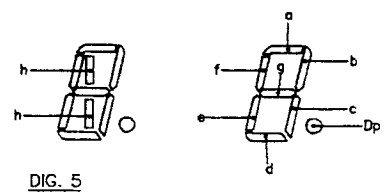


DIG. 1



GRID ASSIGNMENT

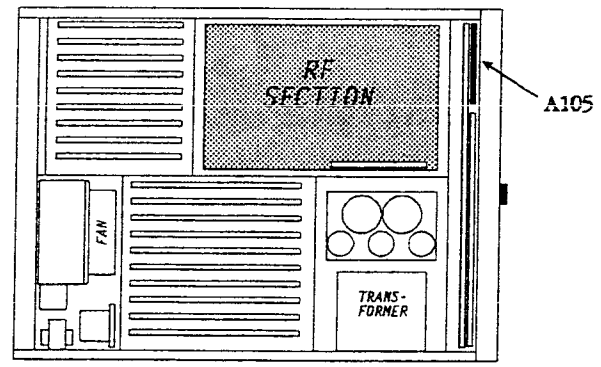




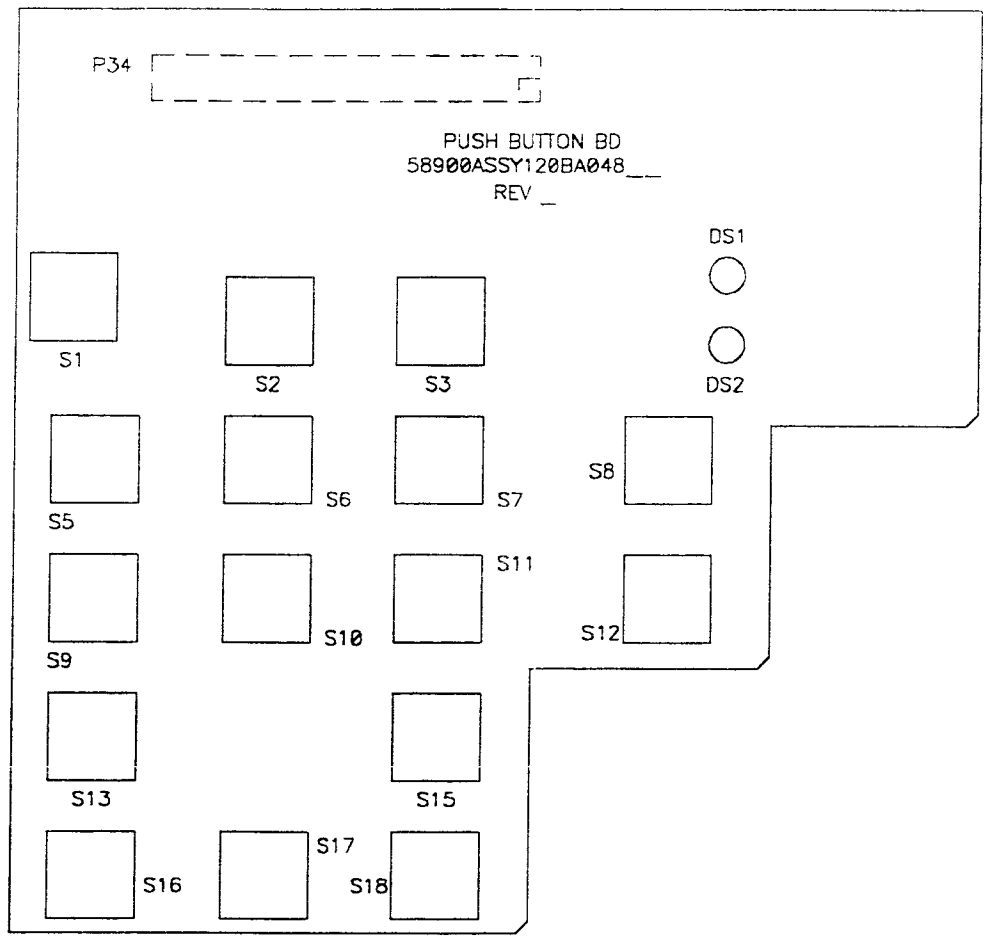
DIG. 5

DIG 1 thru 5

5 & 9 Digit Display (A104)
DWG# 120BM05600 Rev C
Sheet 1 of 1
7-A104-1



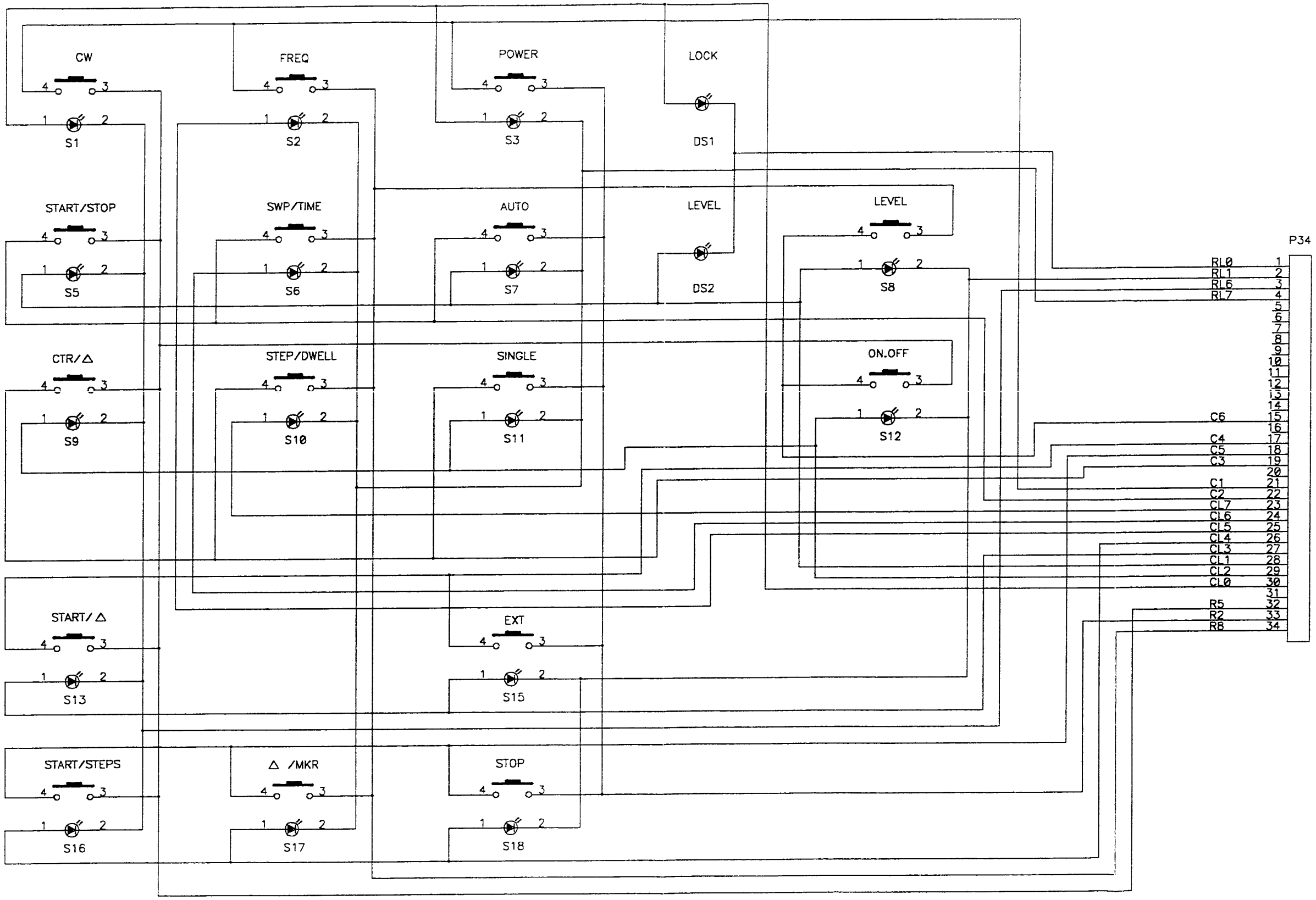
Pushbutton (A105)
ASSY# 120BA04801 Rev C
Sheet 1 of 3
7-A105-1



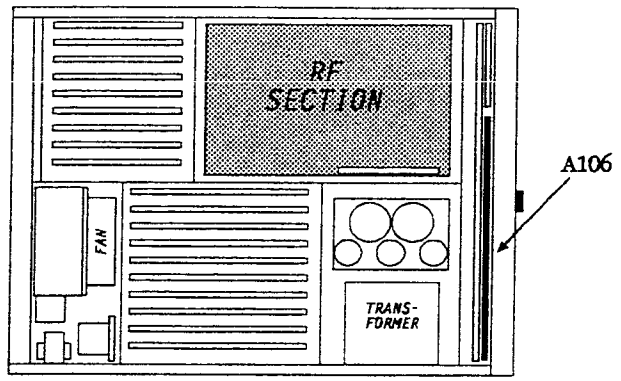
PUSH BUTTON -- PC ASSY A105

The Push Button board holds the push buttons for the sweep functions, the level buttons and their corresponding LEDs as well as the LOCK and LEVEL LEDs.

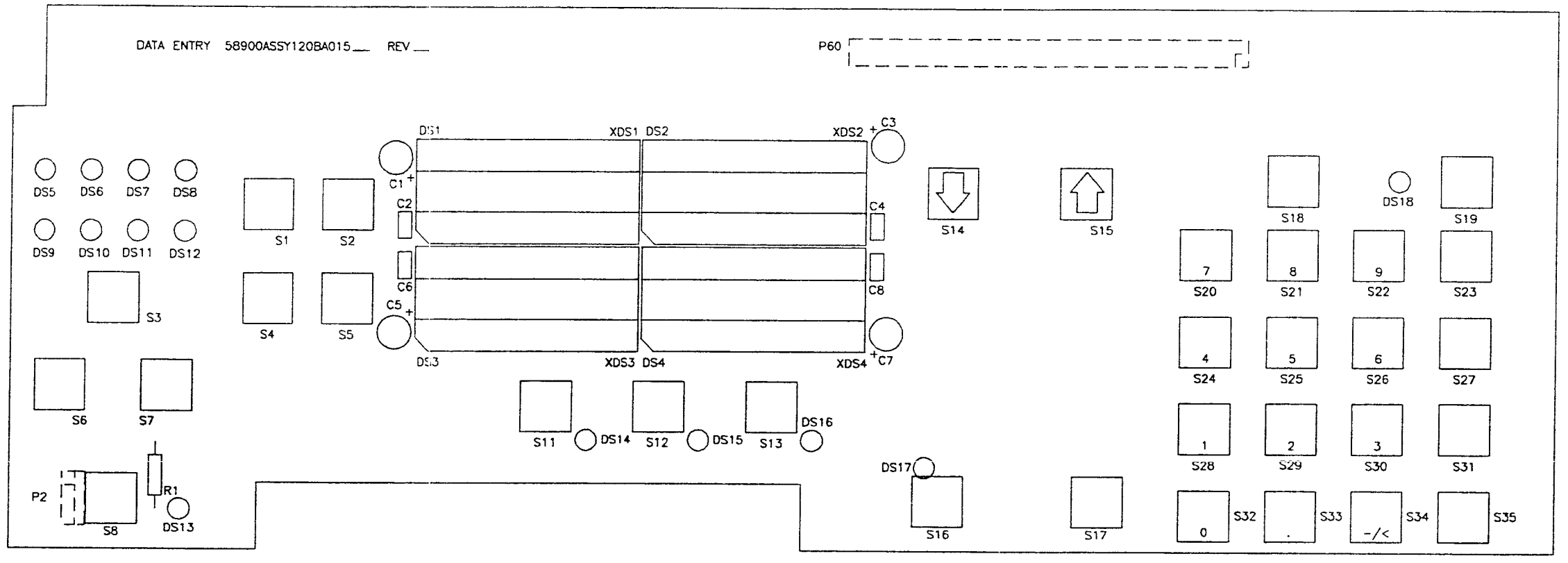
The buttons are connected together such that they can be read and identified using a row and column scheme. The LEDs are set up the same way using a row and column scheme (denoted RL and CL) to light the appropriate LEDs.



Pushbutton (A105)
ASSY# 120BA04801 Rev C
Sheet 3 of 3
7-A105-3



Data Entry (A106)
DWG# 120BM01511 Rev B
Sheet 1 of 4
7-A106-1



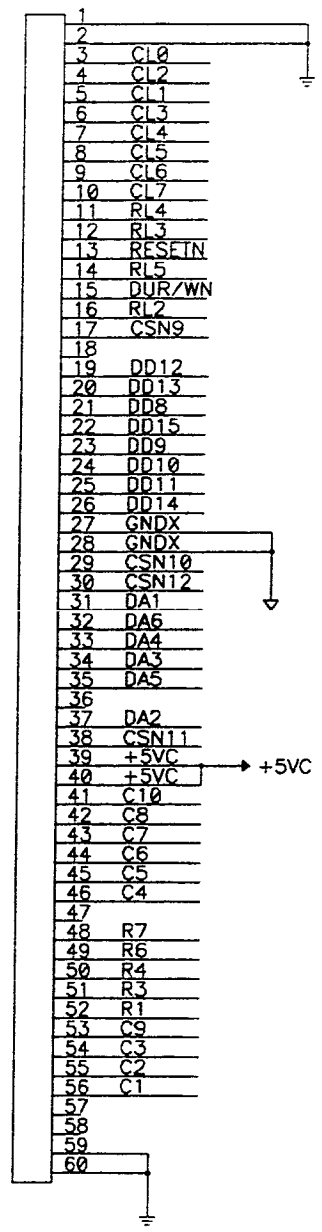
DATA ENTRY -- PC ASSY A106

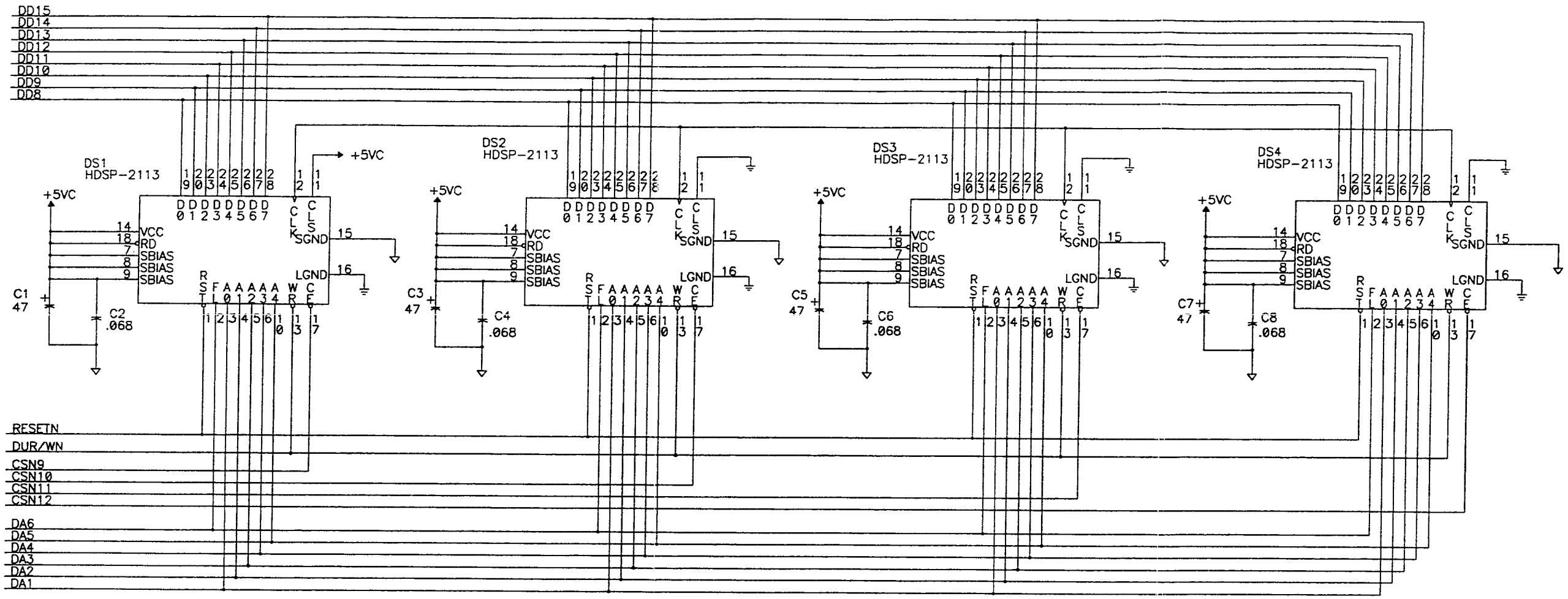
This board holds the push buttons for the keypad, modulation buttons and the sweep marker buttons, as well as any corresponding LEDs. In addition the Intelligent HP alpha numeric displays reside on this board.

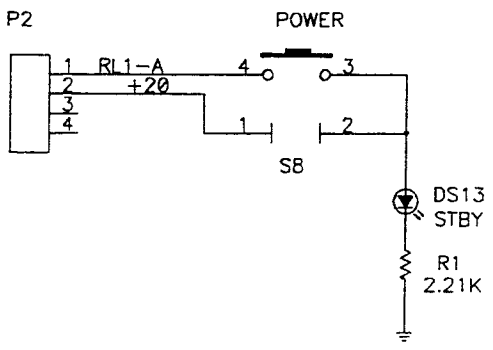
As on the Push Button Board A105, the push buttons are read and the LEDs are lit using the rows and columns scheme. The four, 8-digit Intelligent HP alpha numeric displays (DS1-DS4) receive address and data information from the display driver board.

When the unit has power applied to it the standby LED DS13 is lit by the 20V from the power supply via P2. When the power switch is activated the 20V coming in on P2 is switched to energize the power relay switch which supplies power to the rest of the unit.

P60:A FROM DISPLAY DRIVER PCB

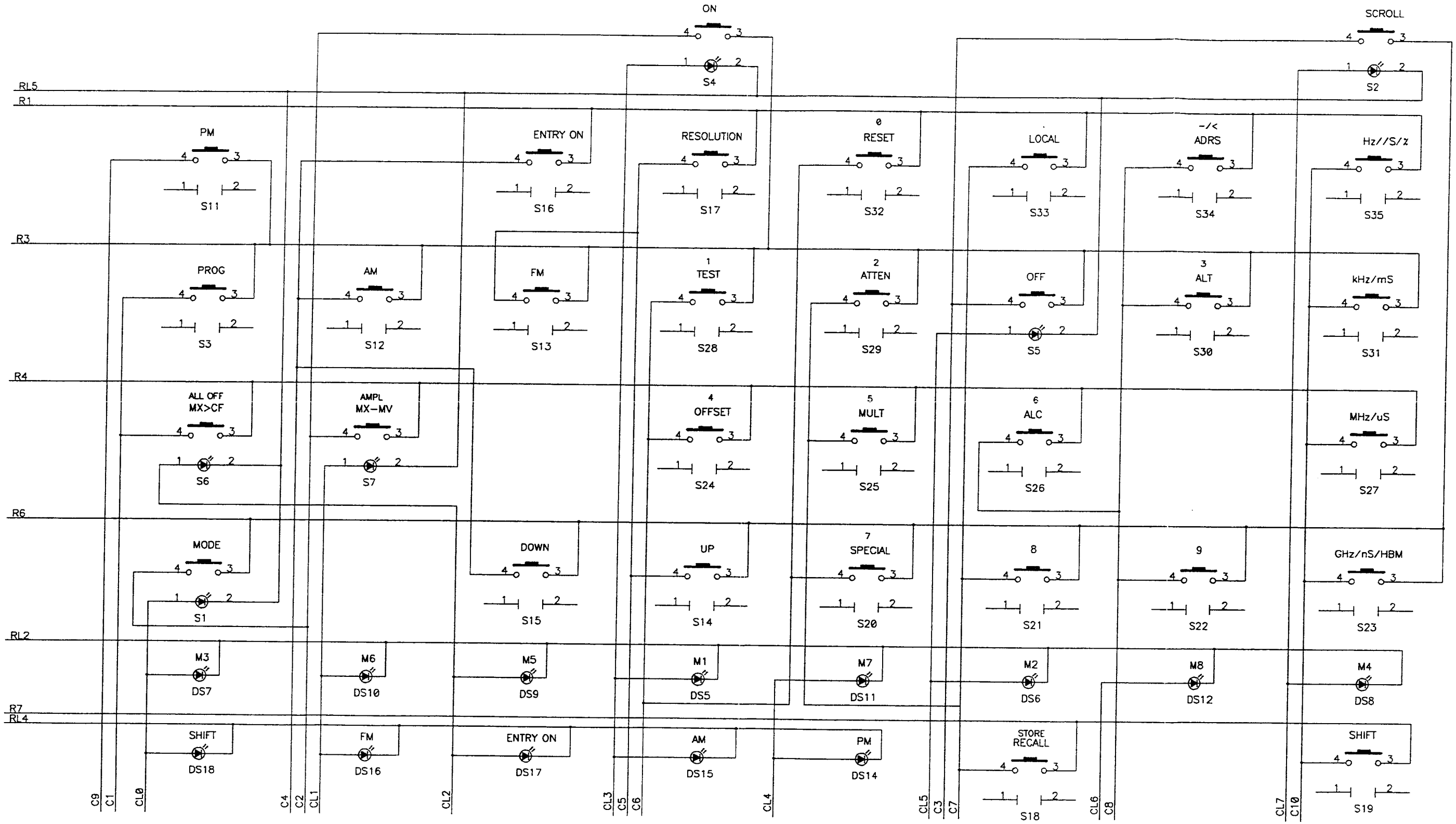






NOTES: UNLESS OTHERWISE SPECIFIED

1. GNDX INDICATES GROUNDED TO CHASSIS.
2. SELN73 (A8–A11) FROM A1.
3. ALL CAPACITORS ARE IN MICROFARADS.



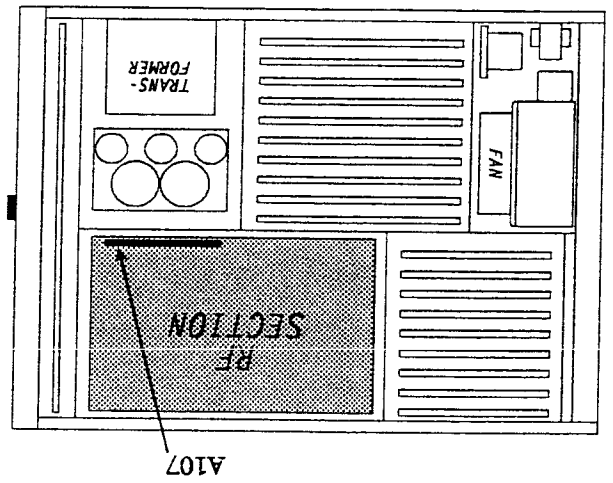
Data Entry (A106)
DWG# 120BM01511 Rev B
Sheet 4 of 4
7-A106-4

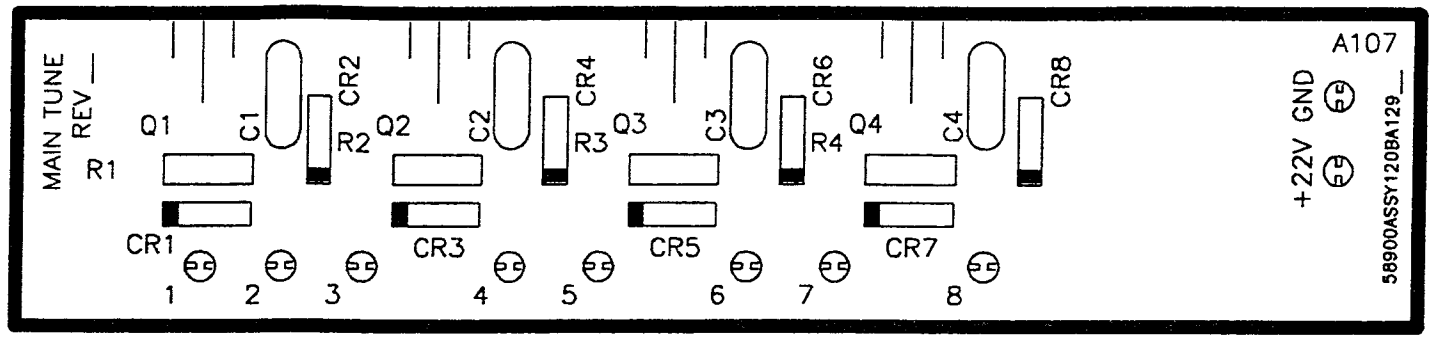
Main Tune (A107)

DWG# 120BM12900 Rev A

Sheet 1 of 2

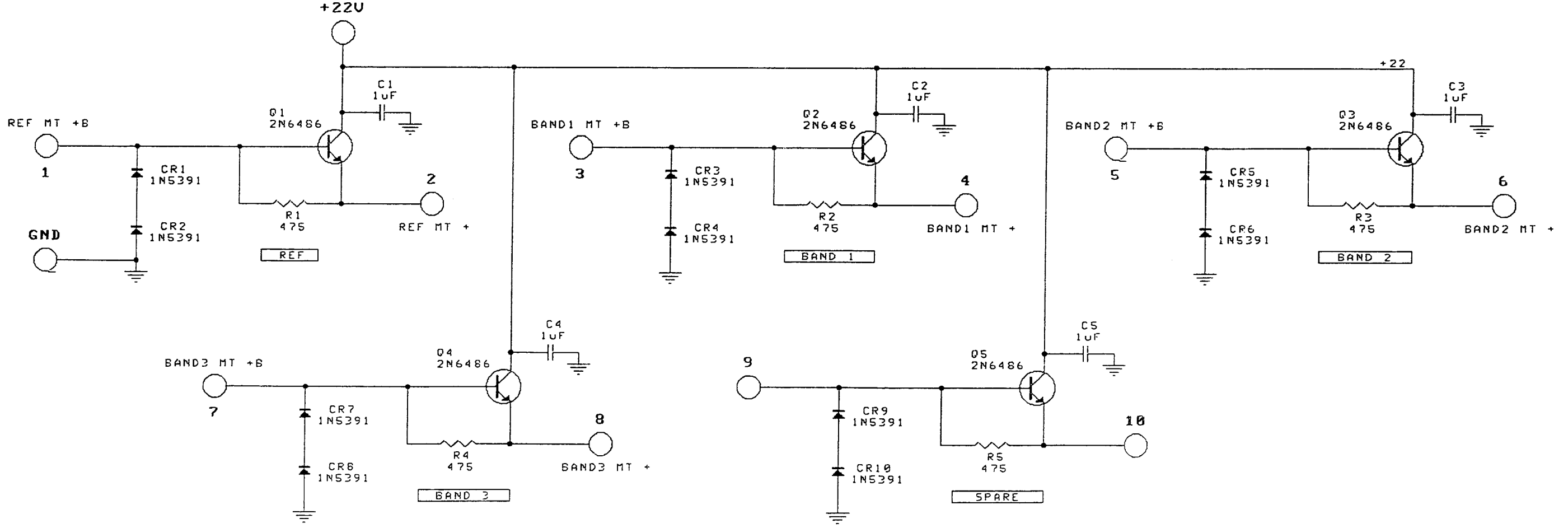
7-A107-1



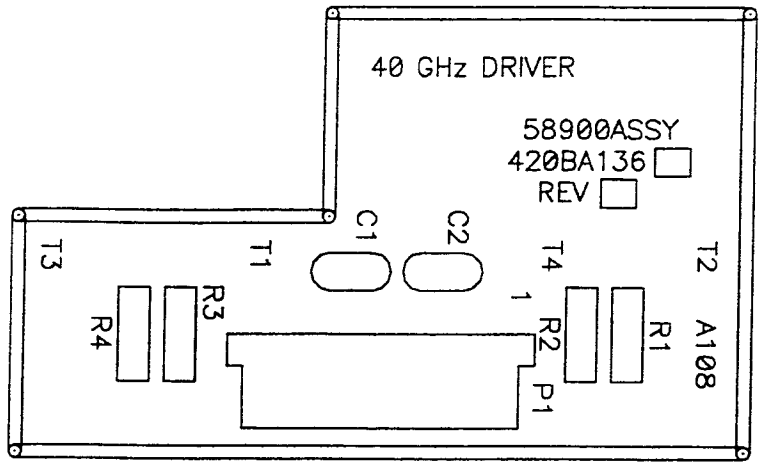


MAIN TUNE -- PC ASSY A107

This circuit board is mounted on the chassis below the Microwave Deck. The board holds the transistors which actually provide the current drive to the Main Tune coils of each of the YIG oscillators. These transistors must provide high currents, resulting in substantial power dissipation which requires the transistors to have a heat sink. The diodes at the base of each transistor are there to prevent the voltage from going too far negative.



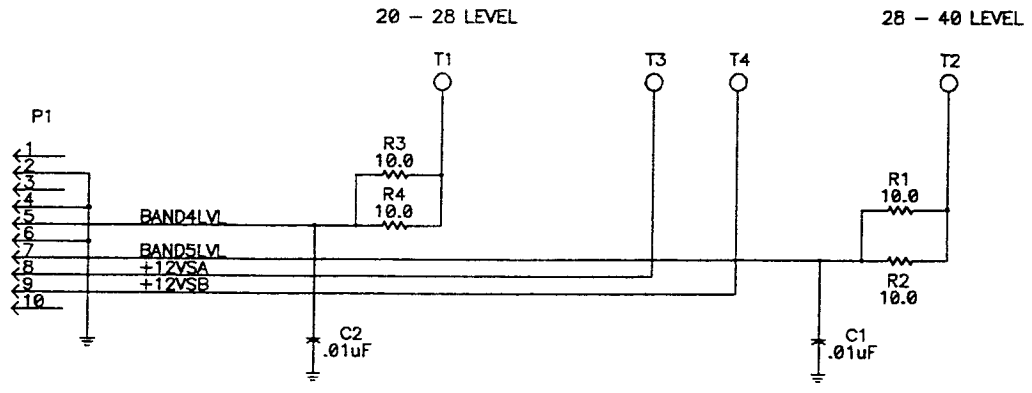
Main Tune (A107)
DWG# 120BM12900 Rev A
Sheet 2 of 2
7-A107-2



40 GHz DRIVER -- PC ASSY A108

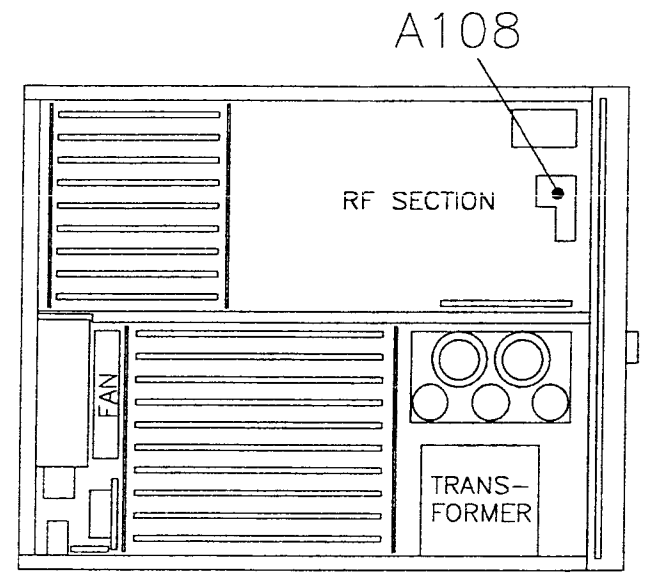
This circuit is part of the level control system in instruments to 40 GHz.

Two leveling inputs are received from the Level board. 'BAND4LVL' controls the 20-28 GHz band; R3 and R4 buffer the 20-28 GHz frequency doubler's level input. 'BAND5LVL' controls the 28-40 GHz band; R1 and R2 buffer the 28-40 frequency doubler's level input. The multi-pin connector (P1) provides connections between the level control system and the frequency doublers.

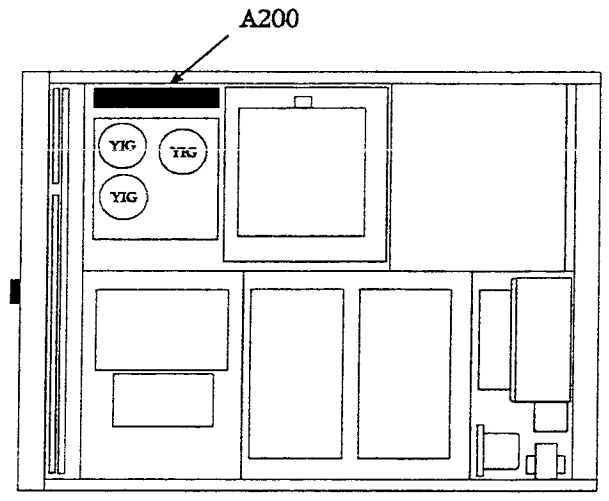


NOTES: UNLESS OTHERWISE SPECIFIED

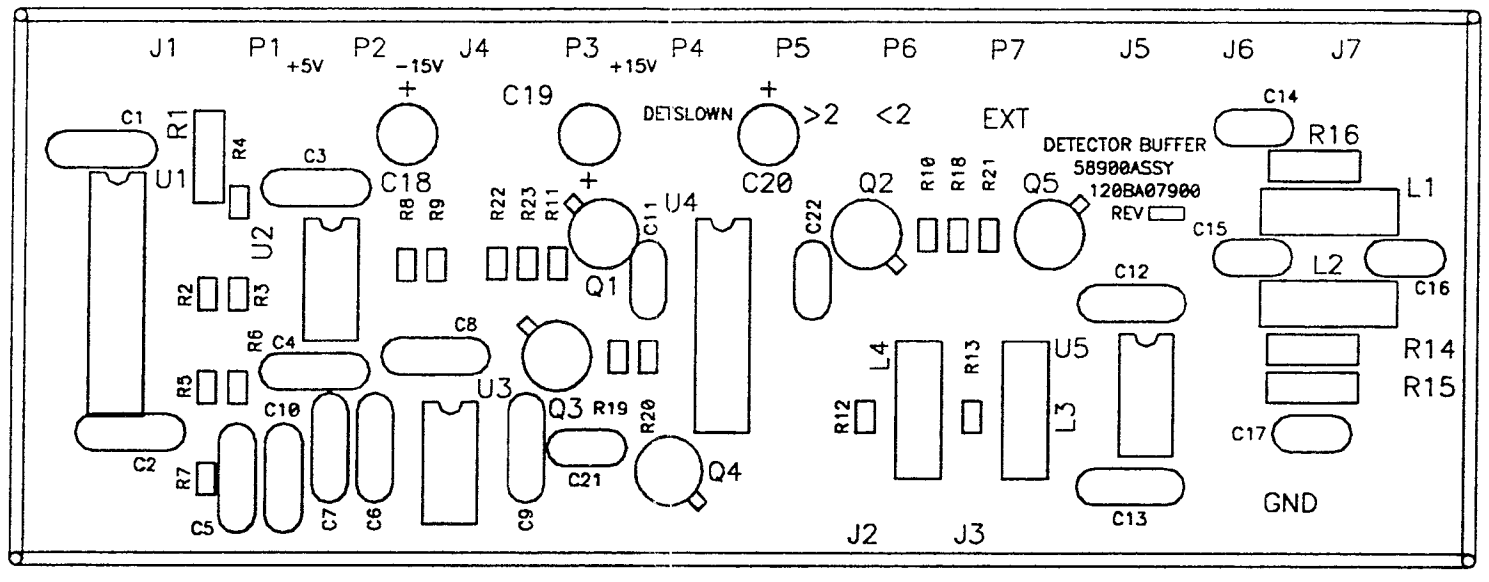
1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/4W, 1%



40 GHz Driver (A108)
DWG# 420BM13610 Rev A
Sheet 1 of 1
7-A108-1



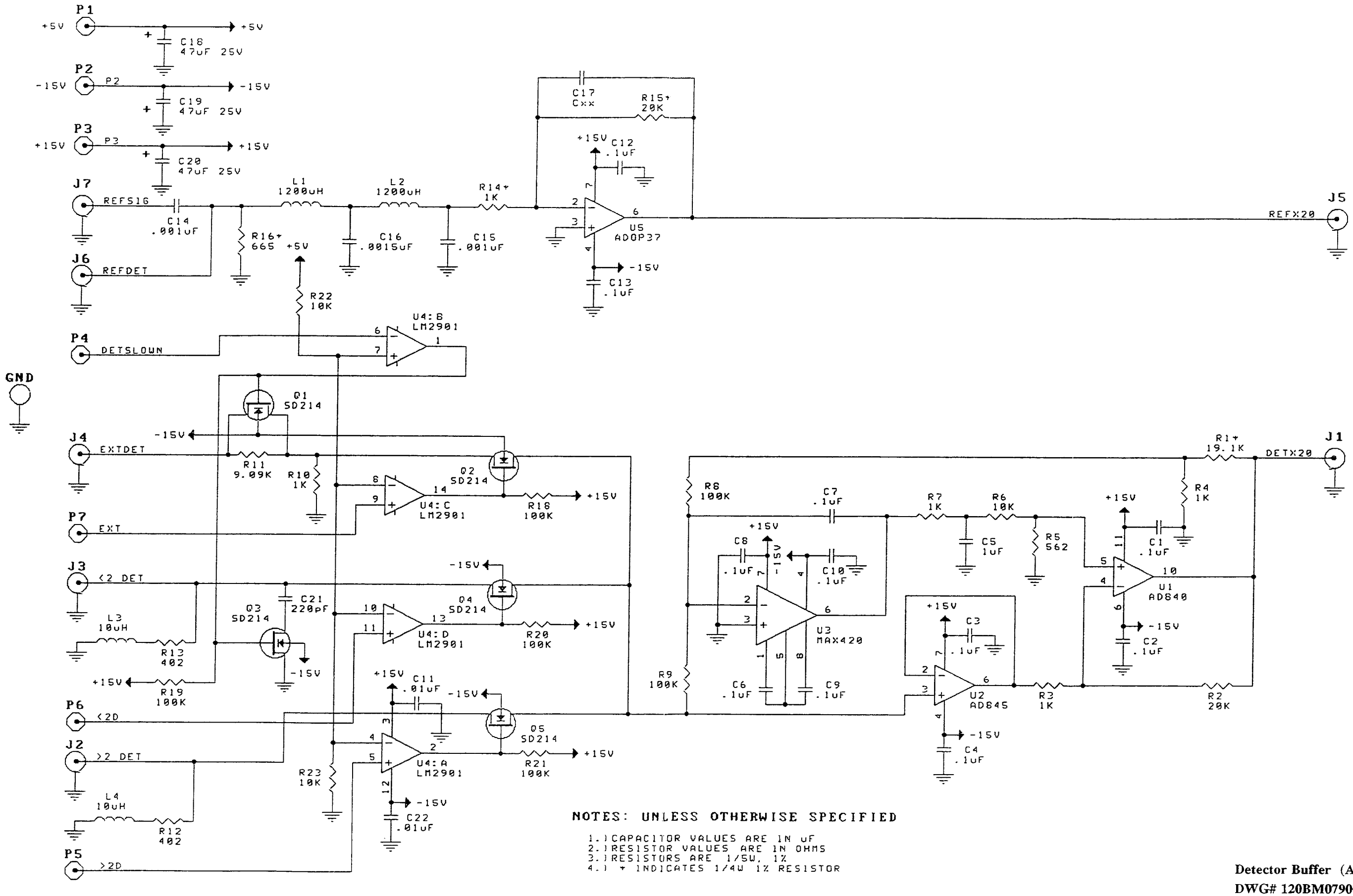
Detector Buffer (A200)
DWG# 120BM07900 Rev D
Sheet 1 of 3
7-A200-1



DETECTOR BUFFER -- PC ASSY A200

The Detector Buffer module is an important part of the leveling system. The 2.5 MHz Reference signal is received from the level board (A10) at J7. This signal is detected by a detector at J6 and a DC voltage proportional to the power level of the reference signal is returned. L1, L2, C15 and C16 filter the reference signal from the DC voltage returned from the detector which is then amplified by U5 and returned to the leveling board thru J5.

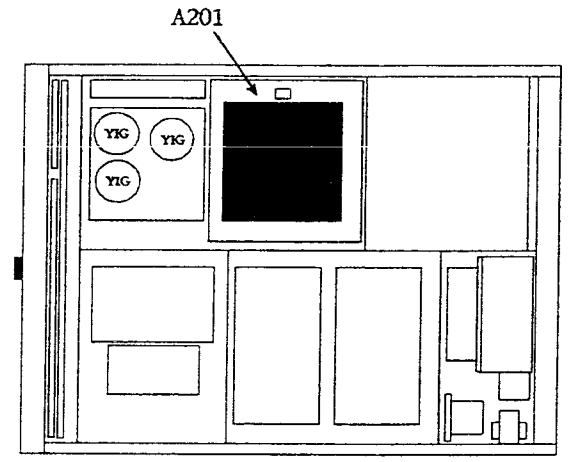
The detector inputs for leveling the instrument's output signal are at J4, J3, J2 which are for an external detector (external ALC mode), the <2 band detector and >2 band detector respectively. The appropriate detector is selected by its respective logic line which switches one of 3 comparators (U4 A, C and D) which in turn switches on one FET Q2, Q4 or Q5. The turned on FET allows the proper detector signal to be fed to the amplifier consisting of U3, U2 and U1. The output is then fed back to the leveling board (A10). The remaining logic signal at P4 serves two purposes. When it is low it turns on the FET Q1 which allows the full voltage of the External Detector signal to be applied to Q2. When the logic is high the External Detector voltage is divided down by a factor of 10. The other function this logic line serves is to switch in a capacitor (when the logic is low) in the <2 path to filter out the RF signal which is coming in on the detector voltage. This logic signal remains low from 10 MHz to 50 MHz and then above 50 MHz it goes high which switches the capacitor out of the <2 detector path.



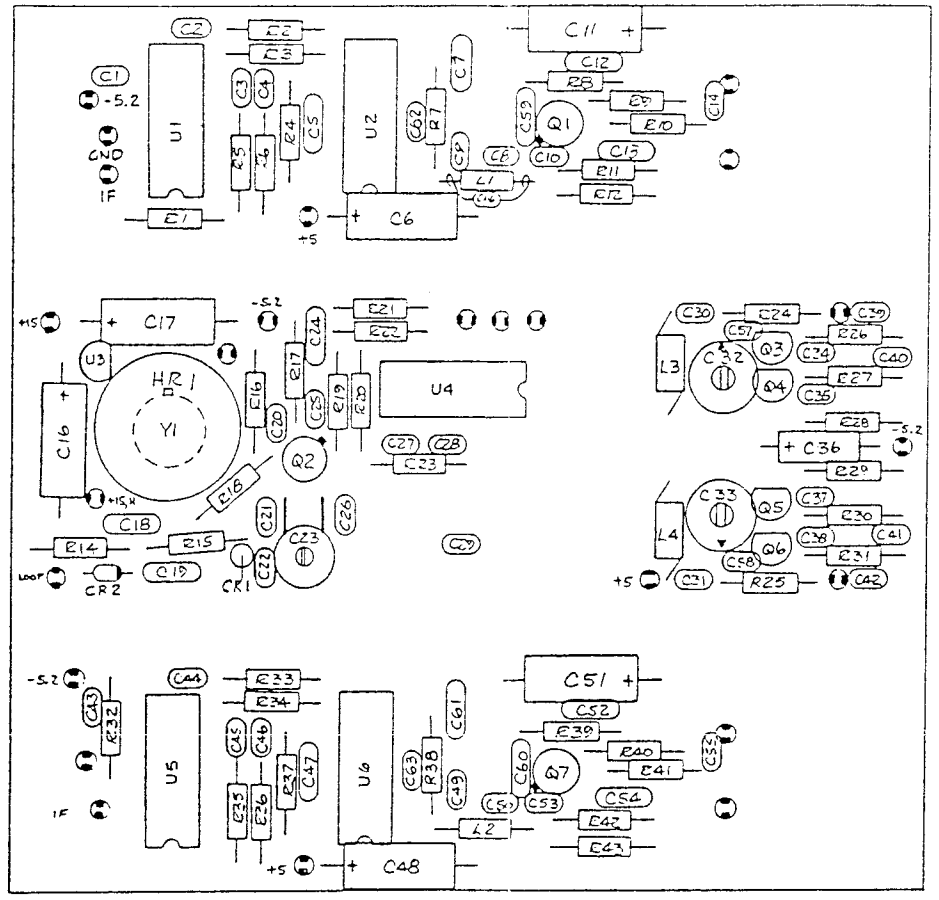
NOTES: UNLESS OTHERWISE SPECIFIED

1.) CAPACITOR VALUES ARE IN uF
2.) RESISTOR VALUES ARE IN OHMS
3.) RESISTORS ARE 1/5W, 1%
4.) * INDICATES 1/4W 1% RESISTOR

Detector Buffer (A200)
DWG# 120BM07900 Rev D
Sheet 3 of 3
7-A200-3



100 MHz Reference Osc (A201)
ASSY# 101CA04200 Rev R



100 MHz Reference Osc (A201)
ASSY# 101CA04200 Rev R
Sheet 2 of 4
7-A201-2

100 MHz OSCILLATOR/SAMPLER DRIVER -- PC ASSY A201

GENERAL

This module includes a 100 MHz Voltage Controlled Crystal Oscillator that is used to drive the sampling mixers, and two identical amplifier circuits that are used to increase the low level IF from those mixers to ECL voltage levels.

100 MHz OSCILLATOR

Transistor Q2, regulated by crystal Y-1, oscillates at a frequency very near 100 MHz. This frequency can be varied slightly by changing the Phase Lock Loop input voltage (and thus changing the capacitance of tuning diode CR1). This variation permits the oscillator to be phase-locked to the Master Reference. In order to bring the oscillator frequency within the relatively narrow adjustment range of the PLL circuit, nominal capacitor C21 is selected during production test, and variable capacitor C23 is adjusted during calibration. With the circuit correctly set up, the 100 MHz loop should become locked with a PLL voltage of +3V DC (this voltage is most easily measured at the Test Point on PC Assy A8, the 100 MHz PLL). Buffer IC4 produces four 100 MHz outputs; two are used to drive the sampling mixers, one returns to the 100 MHz PLL, and one is used to supply a stable 100 MHz reference to the Frequency Counter and/or the 10-12 MHz PLL (1 kHz Resolution Circuit), if installed.

SAMPLER DRIVE

The twin amplifier circuits (Q3-Q4 and Q5-Q6) are used to supply a large (4-6 Vpp) 100 MHz signal to the sampling mixers. Variable capacitors C32 and C33 are used for peaking this signal. The sampling mixers include a step-recovery diode multiplier, which produces numerous harmonics of the 100 MHz input. The RF input to the sampler is mixed with these high frequencies, one of which will be near enough to it in frequency to create an IF that is within the bandwidth of the Sampler IF Amplifier. Example: For an RF input to the sampler of 6905 MHz, the sampler will mix the 69th harmonic of 100 MHz (6900 MHz) with the RF input and produce a 5 MHz IF output.

SAMPLER IF AMPLIFIER

The twin amplifier circuits (Q1-IC2-IC1 and Q7-IC6-IC5) convert the low level IF produced by the samplers to ECL-level signals. Between the transistor amplifier stage and the video amplifier (IC2/IC6) is a low-pass filter that limits the bandwidth to 50 MHz, in order to block undesired high frequencies produced by the mixer. Low frequency noise is blocked by capacitors C62 and C63. The buffers (IC1/IC5) convert the IF to an ECL-level signal for use by the Reference and Fixed L.O. PLL circuits. Typically, this IF is 5 MHz; for output frequencies above 7999 MHz or below 2000 MHz, the Reference Sampler's IF will be 1.667 MHz.

REF. ONLY
MOUNTED ON
SAMPLER ELECTR ASY

U1
7905.2

-15V
C1
1μF
-5.2V

OVEN +15V
C18
1.0
HR1
OVEN
GND

VOLTAGE
REGULATOR
U3
78L12
+15V
C17
10
+12V REG. OUT
C16
10
100 MHz
<.1Vpp

C29
.001
L5
(CHOKE
IMPLEMENTED
IN BOARD
ARTWORK)
C26 4.7pF
100 MHz
2Vpp +12VDC

C21
15pF
NOM.
C23
1-12
R18
10K
(CRYSTAL LOCATED WITHIN OVEN)
Q2
G304
Y1
100 MHz
C25
.001

(FROM AB-U) PLL INPUT
RANGE ~
-5 TO +20V
(FREQUENCY INCREASES
AS VOLTAGE GOES MORE
POSITIVE)
NORMAL PLL
VOLTAGE: +3VDC
R14
10K
R15
22.1K
CR1
MV109
C22
33pF
C20
33pF
R16
4.75K
R17
562
CR2
2810
C19
1
R23
1.3K
C28
.001

R19
6.81K NOM.
100 MHz
AT ECL LEVELS
C27
10pF
U4
100 MHz
ECL LEVELS
R21
332
R22
332
R20
3.92K
-5.2V

(100MHz REF. FOR
COUNTER AND/OR
1KHz RES. CKT.)
TO A105 J2
OR A108 J3
U4
100 MHz
ECL LEVELS
(100MHz REF.
FOR PLL)
TO A8-5

-5.2V
C2 .001
C7 1.0
C11 +10
C24 1.0
C36 +10
C40 .001
C41 .001
C44 .001
C51 +10
C61 1.0
-5.2V

+5V
C5 1.0
C6 +10
C12 1.0
C30 .001
C31 .001
C47 1.0
C48 +10
C52 1.0
+5V

NOTES:
UNLESS OTHERWISE NOTED:
1.) RESISTORS IN OHMS
2.) CAPACITORS IN μF

IC #	TYPE	PIN # -5.2V	PIN # GND	PIN # +5V
1, 4, 5	10216	8	1-16	—
2, 6	UA733	5	—	10

100 MHz ECL LEVELS
(LOADED DOWN)

+5V
L6
27μH
L3
A≅10
C32
9-35
100 MHz
4-6Vpp
+5VDC
C57
47pF
C39
68pF
R24
150
100 MHz
4-6VDC
A
TO SAMPLER
SEE SHT. 2

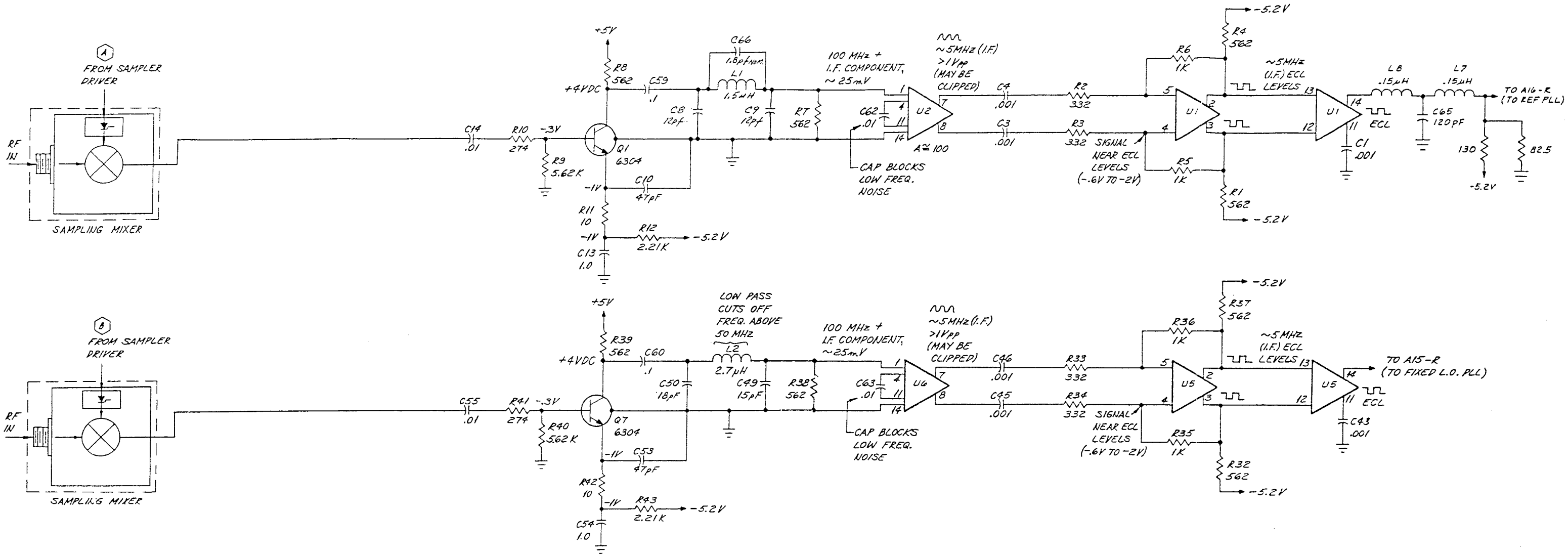
Q3
4275
Q4
4275
-2V
C34
.001
C35
.001
R28
332
R26
100
R27
100
-5.2V

100 MHz ECL LEVELS
(LOADED DOWN)

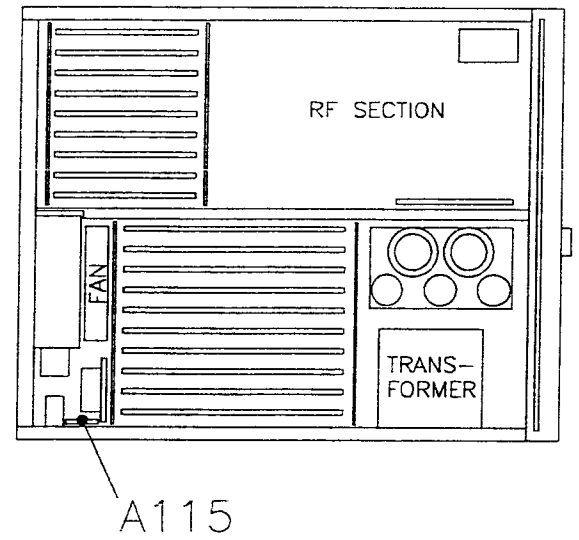
L4
A≅10
C33
9-35
100 MHz
4-6Vpp
+5VDC
C58
47pF
C42
68pF
R25
150
100 MHz
4-6VDC
B
TO SAMPLER
SEE SHT. 2

Q5
4275
Q6
4275
-2V
C37
.001
C38
.001
R29
332
R30
100
R31
100
-5.2V

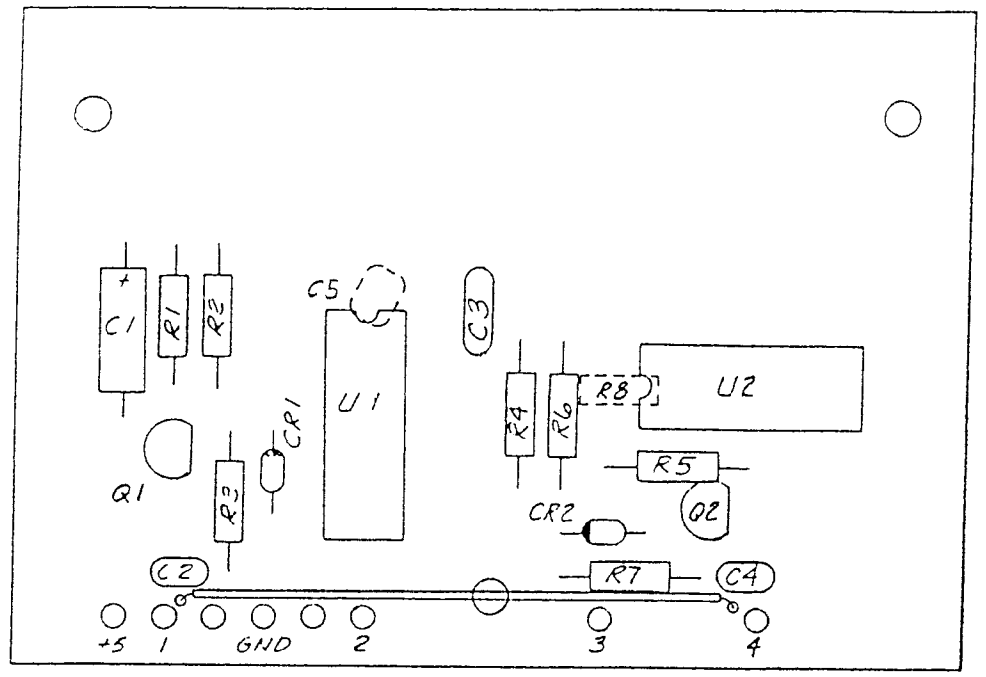
100 MHz Reference Osc (A201)
ASSY# 101CA04200 Rev R
Sheet 3 of 4
7-A201-3

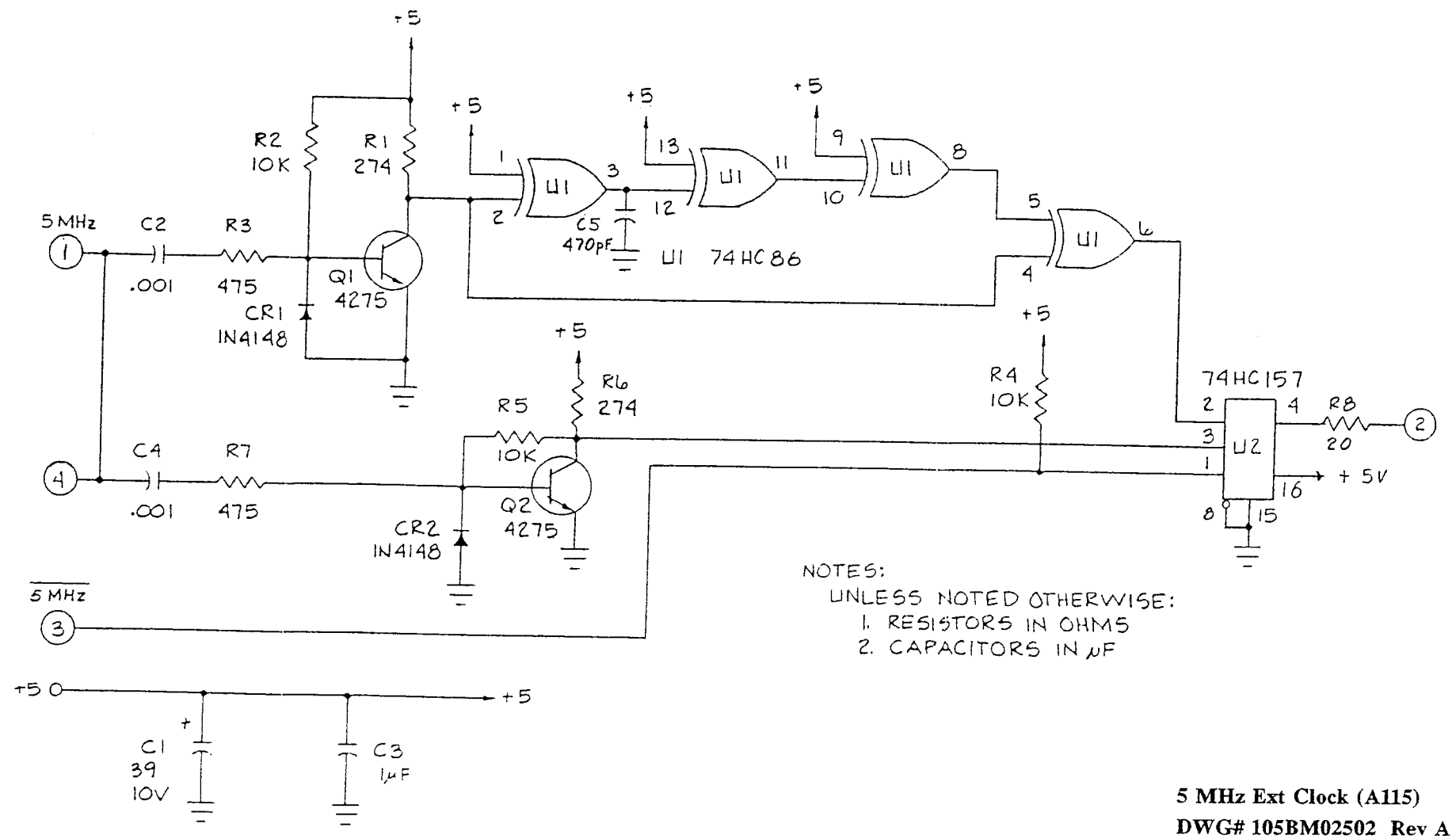


100 MHz Reference Osc (A201)
ASSY# 101CA04200 Rev R
Sheet 4 of 4
7-A201-4

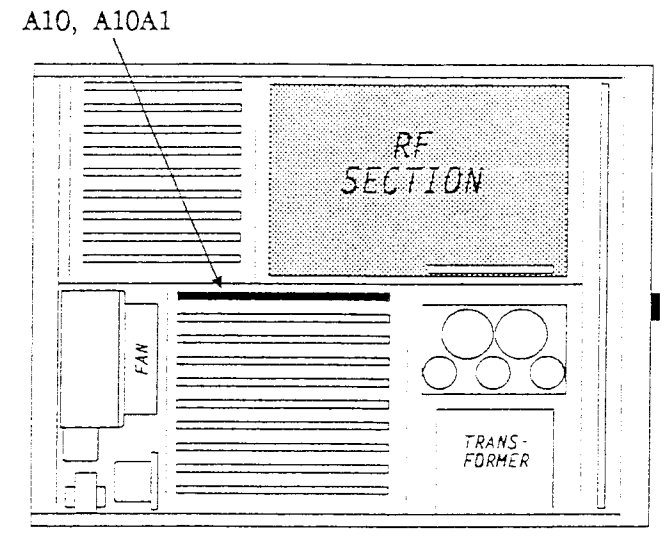


5 MHz Ext Clock (A115)
DWG# 105BM02502 Rev A
Sheet 1 of 2
7-A115-1

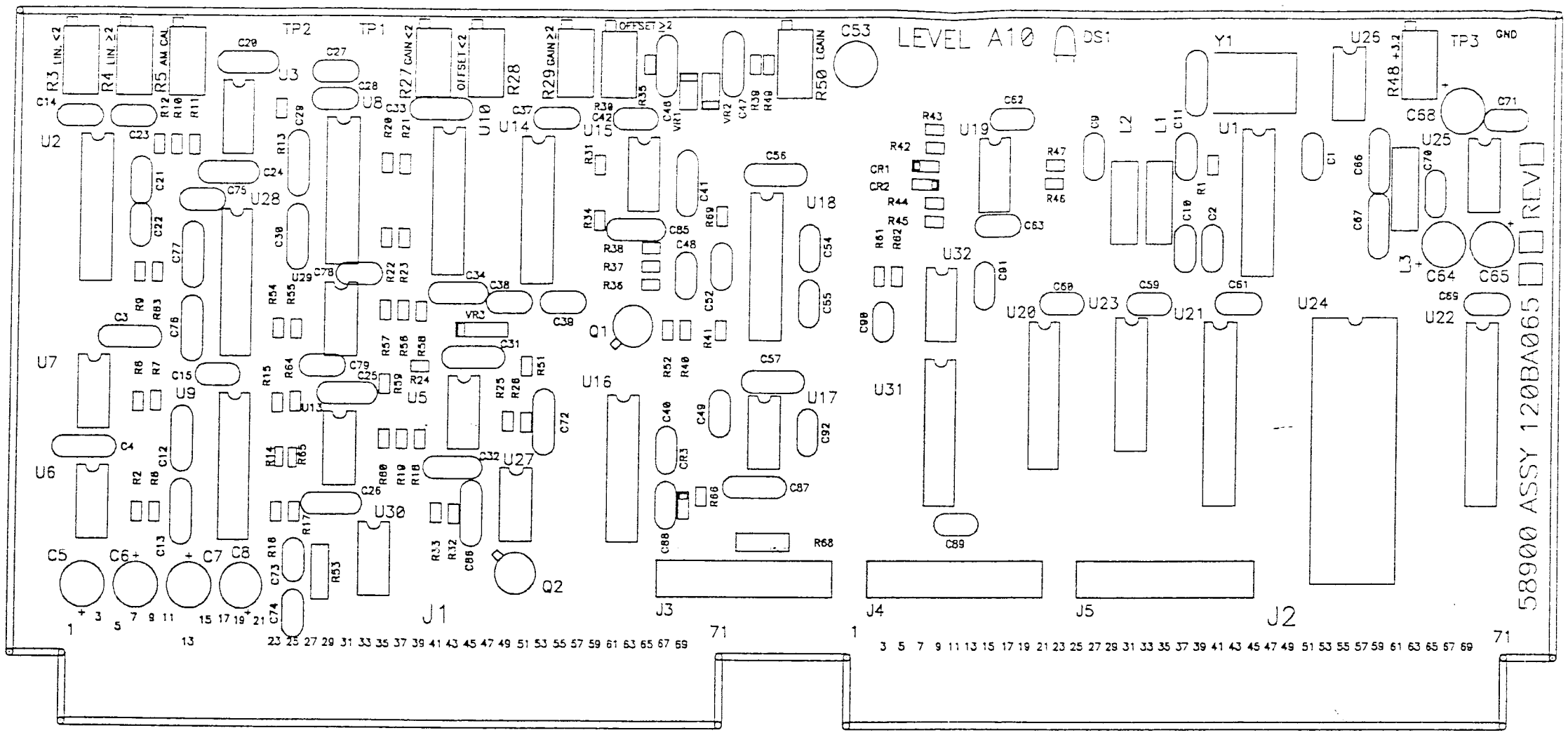




5 MHz Ext Clock (A115)
DWG# 105BM02502 Rev A
Sheet 2 of 2
7-A115-2



Level (A10)
ASSY# 120BA06510 Rev E
Sheet 1 of 5
7-A10-1



LEVEL – PC ASSY A10

The leveling scheme used in the 7000 series can be compared to a Frequency Locked Loop. The similarities are that the leveling loop has a reference and a variable input which are compared and the loop action adjusts the variable input (which is proportional to the actual unit output level) until the two inputs are balanced. The comparison is made at the summing junction of an op amp integrator; the output of the integrator is used to control pin leveling diodes which adjust the RF power level. This power level is detected and amplified as required and is returned as the variable input to the integrator.

On this board U17 A is the op amp integrator whose summing junction at pin 2 is comparing a reference input and the detected RF input. The reference input is the REFX20 input from the detector buffer module A200 which is amplified by U15. The gain is adjustable via pots R27 (GAIN <2 for downconverter frequencies) and R29 (GAIN >2 for frequencies >2GHz) and is switched by U14 A and B depending on the instrument's output frequency. The variable input to the U17 summing junction is the actual RF detector voltage which has been amplified at the detector buffer module A200. Q2 samples this signal (DETX20) when the unit is pulse modulated. When the unit is not pulse modulated, Q2 is turned on and the detector voltage, buffered by U30, can be inverted by U27, depending on whether the detector voltage is negative or positive. This inversion is controlled by switch U16 A and B. In addition to these two inputs to the summing junction of U17, offset voltages are summed in as well. Two different adjustable offsets (R28 and R30) are available and are switched by U14 C and D depending on whether the output frequency is > or <2 GHz. Q1 samples the signals at this summing point when in pulse modulation mode or, if pulse is turned off, Q1 is turned on all of the time. The summing integrator U17 A has variable feedback paths available. U18 A, B, C and D are switched in as appropriate for different leveling modes. The output of the amplifier is fed to U19 via CR1 and CR2; this serves as a window detector to detect when the leveling loop is unleveled. When the loop is unleveled U19-7 goes low, lighting DS1 and sending a low logic signal to the computer. The output of the U17 A amplifier is also amplified by U17 B, whose gain is variable via R50 (LGAIN) pot. The output of U17 B is the level voltage which goes to the level driver board (A10A1) which ultimately drives the pin leveling diodes.

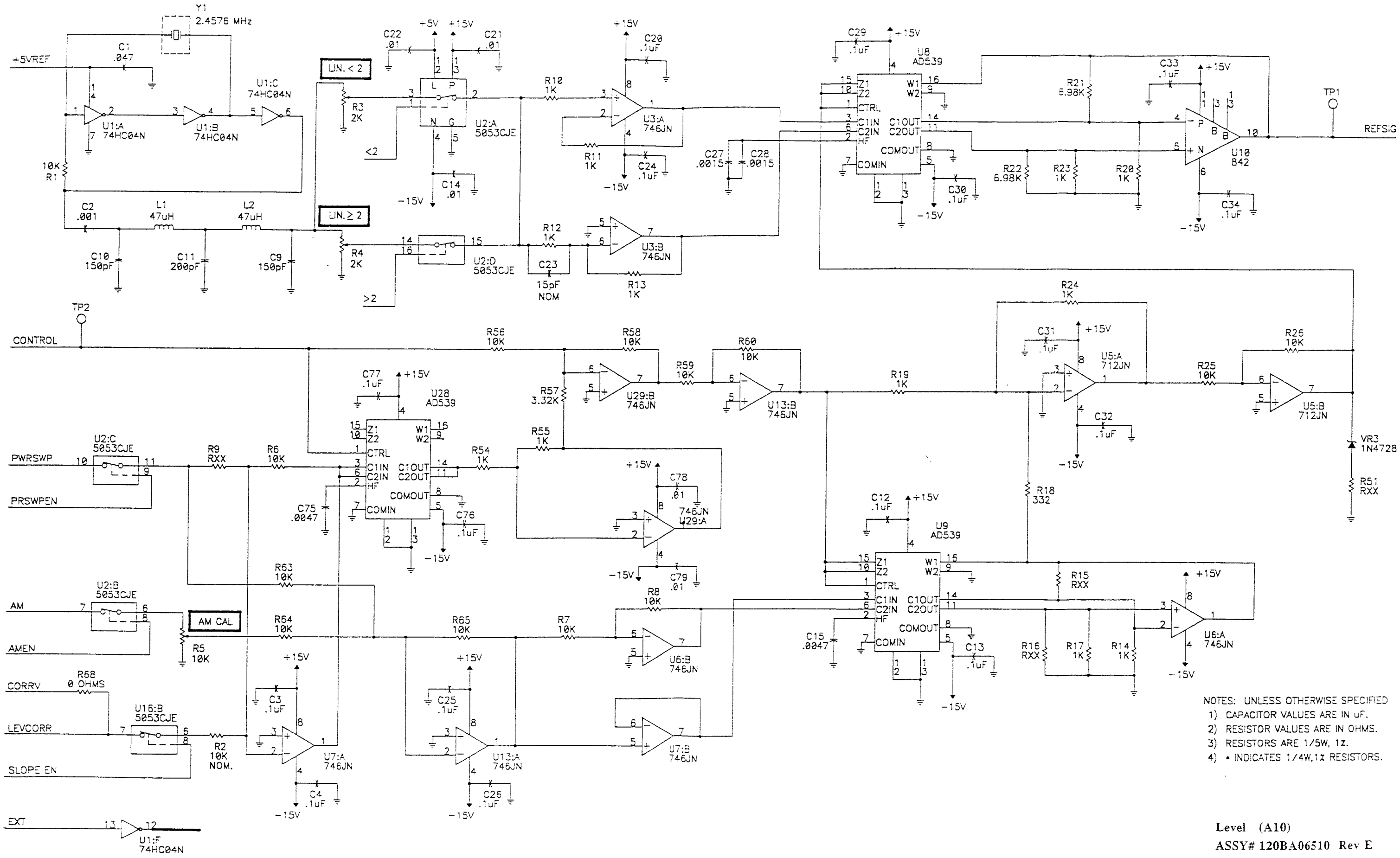
The reference signal is generated on this PCA. The 2.4596 MHz oscillator is composed of U1 A, B, C and Y1; its square wave output is then turned into a sine wave via filter L1, L2, C10, C11 and C9. R3 and R4 pots allow a variable amplitude of this signal to be tapped off and amplified. U2 A and B switch in the appropriate pot dependant on whether the frequency selected is > or < 2 GHz. The signal is translated into a differential signal and fed to a modulator U8 (which functions as a variable attenuator) controlled by a voltage which may be a composite of different signals. The output of the modulator is combined by U10 and is output to the Detector Buffer module to be amplified and returned to the leveling board as REFX20.

The main control voltage for the modulator IC's (U8, U28 and U9) is generated by the DAC U24. This voltage changes as the power level changes and is used to control the gain of U28. U28 adjusts the level correction voltage which is switched in by U16 D and amplified by U7 A. If power sweep is activated the power sweep ramp is enabled by U2 C and is also amplified by U7 A. The amplitude of these two signals is adjusted by the modulator U28 according to the power level the instrument is set to. U29 A amplifies the modulator output and sums it with the standard main control voltage at U29 B. The output of U29 B is inverted at U13 B and is used to control the modulator U9 which adjusts the amplitude of the AM signal when enabled by U2 D. R5 calibrates the AM signal which is then translated into a differential signal by U6 B and U7 B and applied to the modulator U9 input. The output of U9 is summed together by U6 A and this AM signal's amplitude has been adjusted according to the control voltage. The result is that the AM signal level is correctly calibrated for any power level. This AM signal is then summed together with its control voltage at U5 A and inverted at U5 B forming a composite signal used for appropriately modulating the reference signal at U8. VR3 and R51 are set to limit the control voltage so that it does not over drive the modulator.

U31 is a DAC programmed by the computer to give an output voltage at U32 B. This voltage is the appropriate offset required for the pin leveling diode drivers on the A10A1 level driver board.

The U26 Reference provides a 5 volt reference which is filtered by L3 and C66 and C67. This filtered 5 volt reference is also amplified by U32 A to give a 10 volt reference. The 5 volt reference is also divided down by pot R46 to give a 3.2 v reference.

U20 provides decoding for the chip select lines. U21, U22 and U23 provide the necessary buffers for the bus interface lines.



NOTES: UNLESS OTHERWISE SPECIFIED
1) CAPACITOR VALUES ARE IN uF.
2) RESISTOR VALUES ARE IN OHMS.
3) RESISTORS ARE 1/5W, 1%.
4) * INDICATES 1/4W,1% RESISTORS.

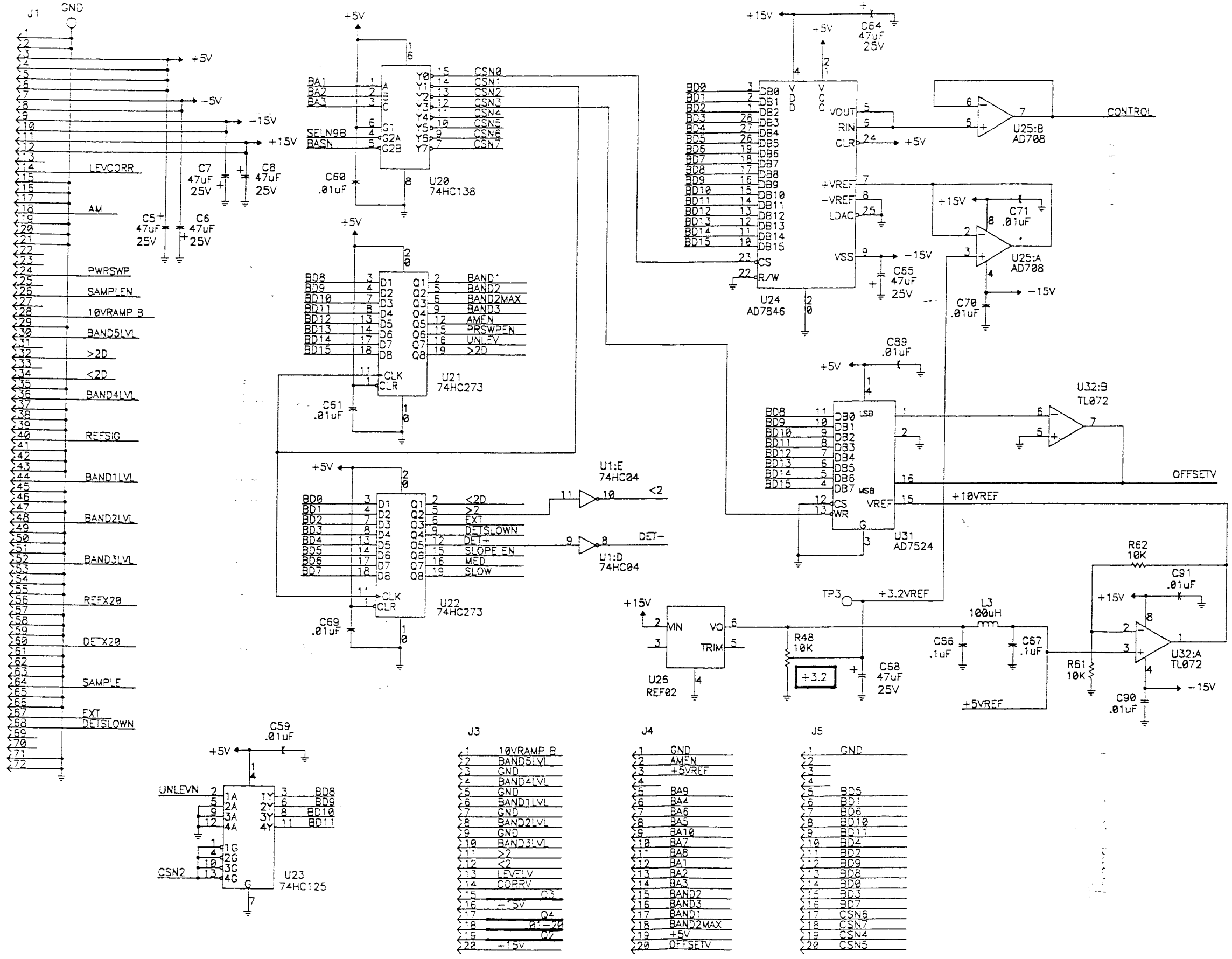
Level (A10)
ASSY# 120BA06510 Rev E
Sheet 3 of 5
7-A10-3

	<20 •		>20	
	AM	CW	AM	CW
.01–20	1	1	0	0
MED	0	1	0	1

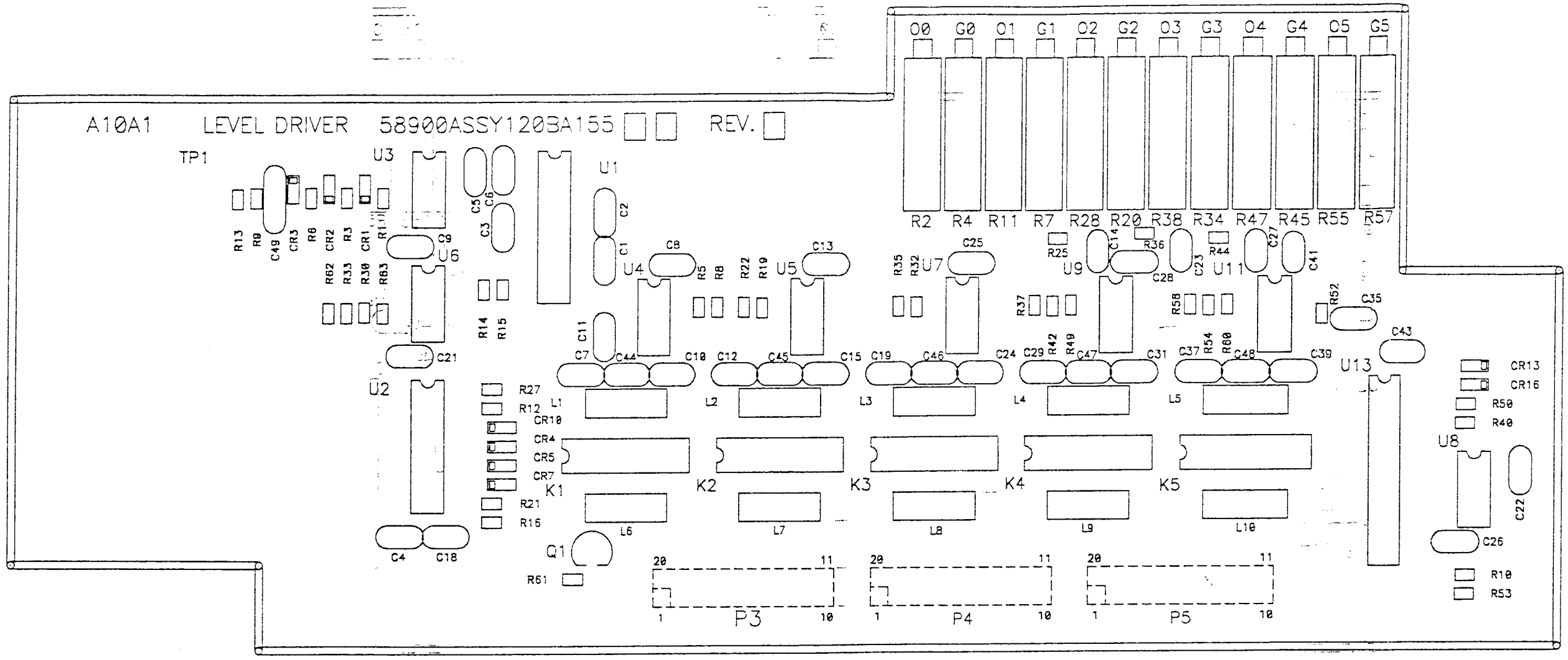
• 20.1 FOR UNITS X TO 20.1 GHZ

U14:D 5053CJE
R27 5K
GAIN <2
<2
+15V +5V
C37 .01
C39 .01
R29 5K
GAIN ≥2
U14:A 5053CJE
C38 .01
≥2
R31 562 NOM
−15V
C42 33pF
C41 .1uF
+15V
REFX20
R34 1K
U15 OP27GN
C85 .1uF
−15V
R38 10K
R66 200K
1M R37
U16:C 5053CJE
UNLEV
R35 1K
+15V
+6.2V
C46 .1uF
VR1 1N827
OFFSET ≥2
R30 10K
R39 1K
−6.2V
−15V
C47 .1uF
VR2 1N827
OFFSET <2
U14:B 5053CJE
R28 10K
>2
<2
−5V
Q1 SD215
R52 100K
−5V
R36 10K
C48 15pF
R40 1.21K NOM
CR3 2810
U17:A 712JN
C57 .1uF
+15V
C49 .001
C87 .1uF
−15V
UNLEV
U18:B 5053CJE
U18:D 5053CJE
MED
U18:C 5053CJE
SLOW
C56 .1uF
C53 33uF 15V_E
R41 2.21K
C92 68pF
R49 10K
R50 50K
LGAIN
R69 2.21K
U17:B 712JN
LEVELV
+5V +15V
C55 .01
C54 .01
SLOW
U18:A 5053CJE
C52 .01
−15V
+5V
R46 1K
DS1 HLMPK101
R47 100K
C62 .01
+15V
CR1 1N4148
CR2 1N4148
U19 311N
UNLEVN
C63 .01
−15V
R45 20K
R43 20K
+15V
−15V
R44 6.98K
R42 6.98K
R33 10K
+15V
C72 .1uF
U27 OP27GN
R32 10K
−5V
Q2 SD215
DETX20
C73 .001
R53 2.21K• NOM
C74 CXX
U30 OP27GN
−15V
+15V
C40 .01
+5V
C88 .01
U16:A 5053CJE
C86 .1uF
−15V
U16:D 5053CJE
SAMPLEN
DET−
DET+
SAMPLE

Level (A10)
ASSY#120BA06510 Rev E
Sheet 4 of 5
7-A10-4

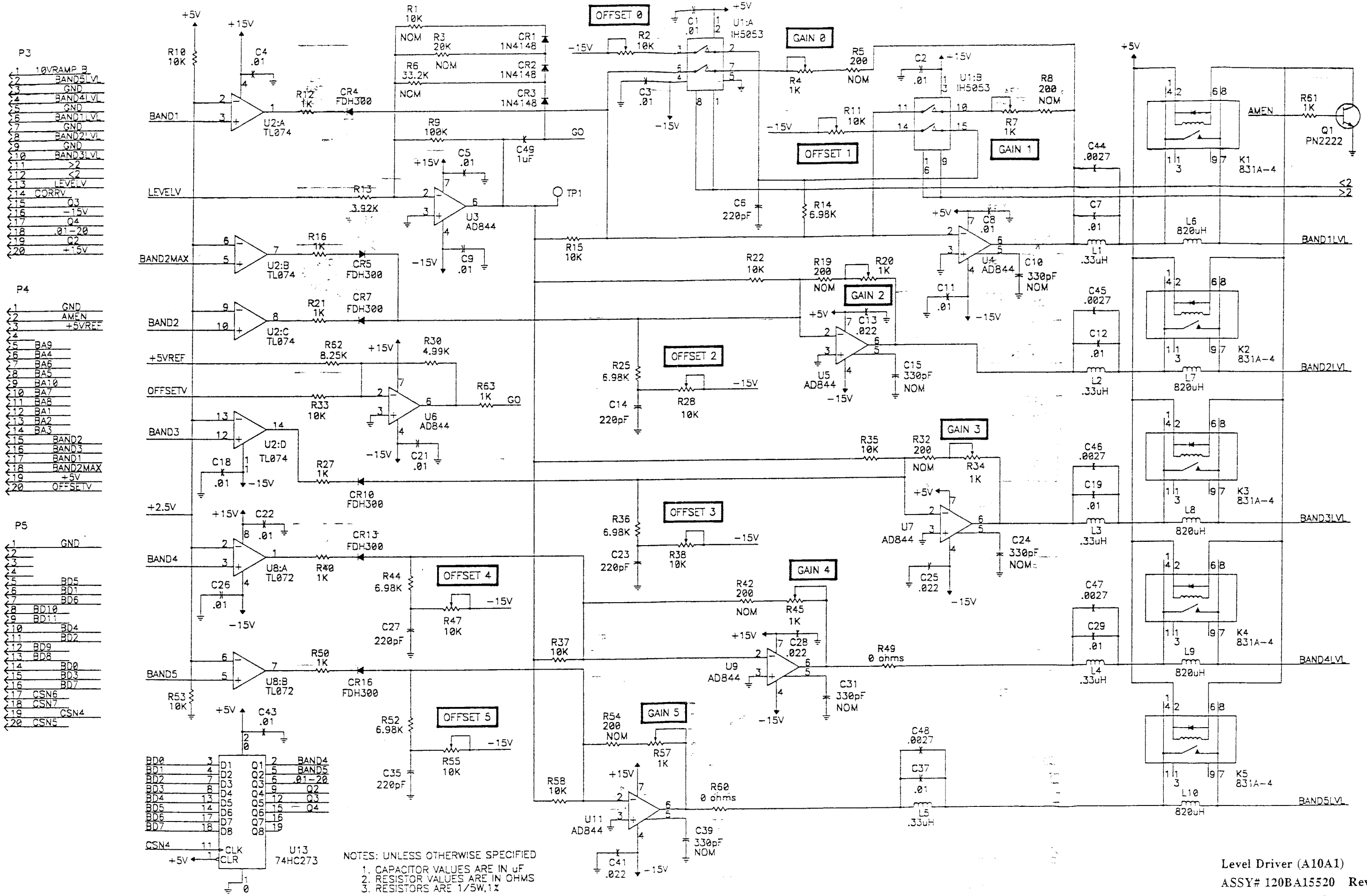


Level (A10)
ASSY#120BA06510 Rev E
Sheet 5 of 5
7-A10-5

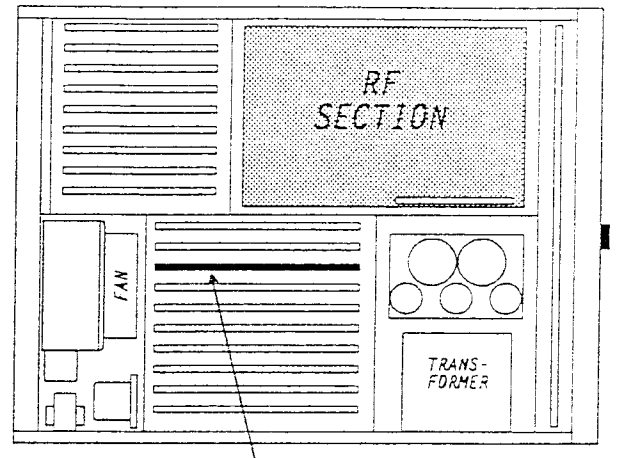


LEVEL DRIVER -- PC ASSY A10A1

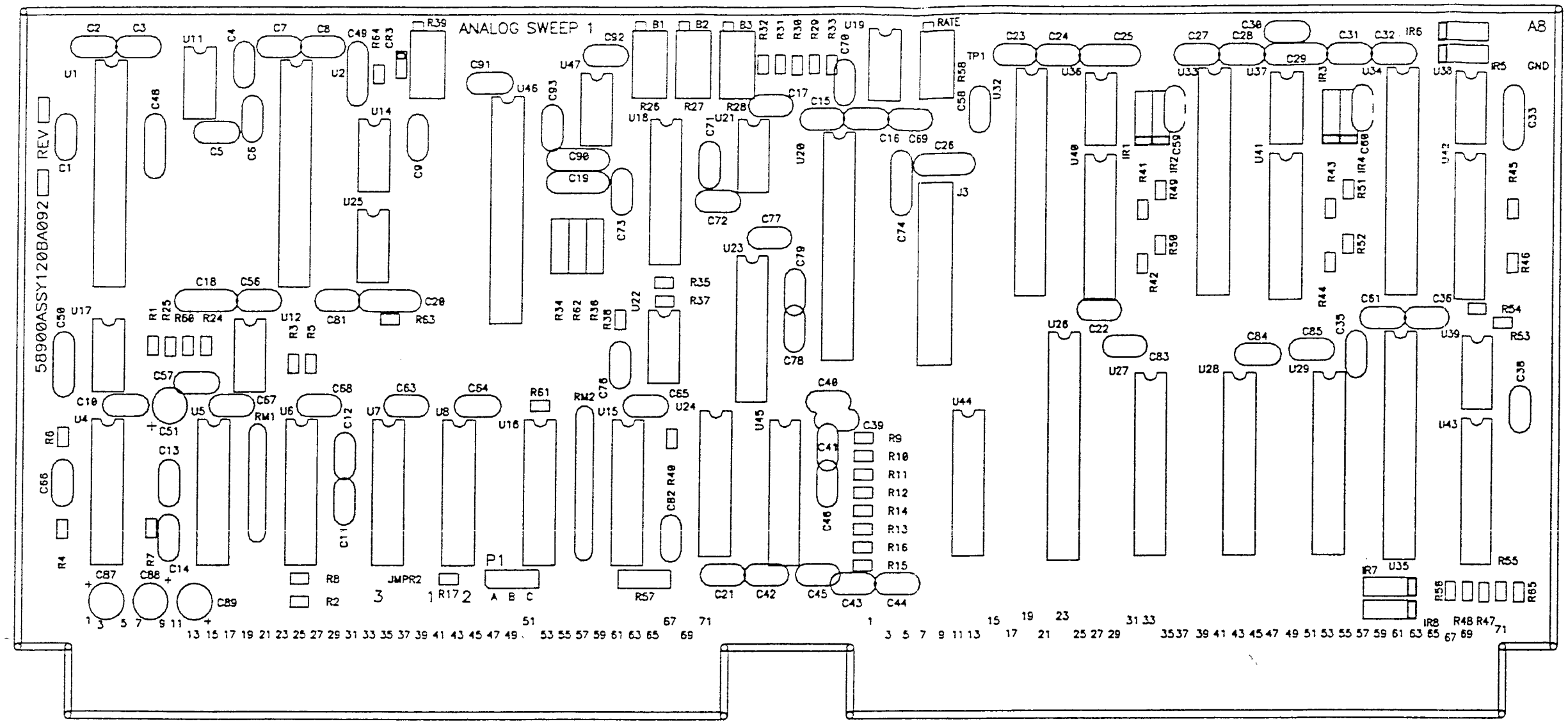
The level driver board holds the circuits which directly drive the PIN diodes leveling circuits inside the RF modules. The level voltage which comes from the A10 level board is applied to the inputs of U3 and U6, which are variable gain amplifiers (their gain is dependent on the level of the input voltage). This variable gain is used to offset the gain change in the leveling loop caused by the leveling diodes. The outputs of U3 and U6 are applied to the summing junction inputs of inverting amplifiers U4, U5, U7, U9, and U11, each of which drives one leveler. Offset voltage inputs from PC board A10, amplified by U2 A through D and U8 A & B, are also applied to these summing junctions. The offset voltages vary, depending on output frequency, in order to keep the variable gain amplifiers within the correct range. The offset voltages are adjustable via pots R2, R11, R28, R38, R47, and R55. U1 changes the gain and offset for U4 when the output frequency is below 2 GHz.



Level Driver (A10A1)
ASSY# 120BA15520 Rev B
Sheet 2 of 2
7-A10-7



A8, A8A1



ANALOG SWEEP #1 – PC ASSY A8

The analog sweep board provides many signals required during analog sweep. The board has DACs which provide ramps for driving the main tune coils of the YIG's, it also has DACs to provide ramp voltages which trigger a number of comparators, thus generating various logic signals necessary to switch various filters and bands. Another set of DACs are used to control comparator reference voltages according to the marker frequencies which may be set. These comparators then generate the marker pulses.

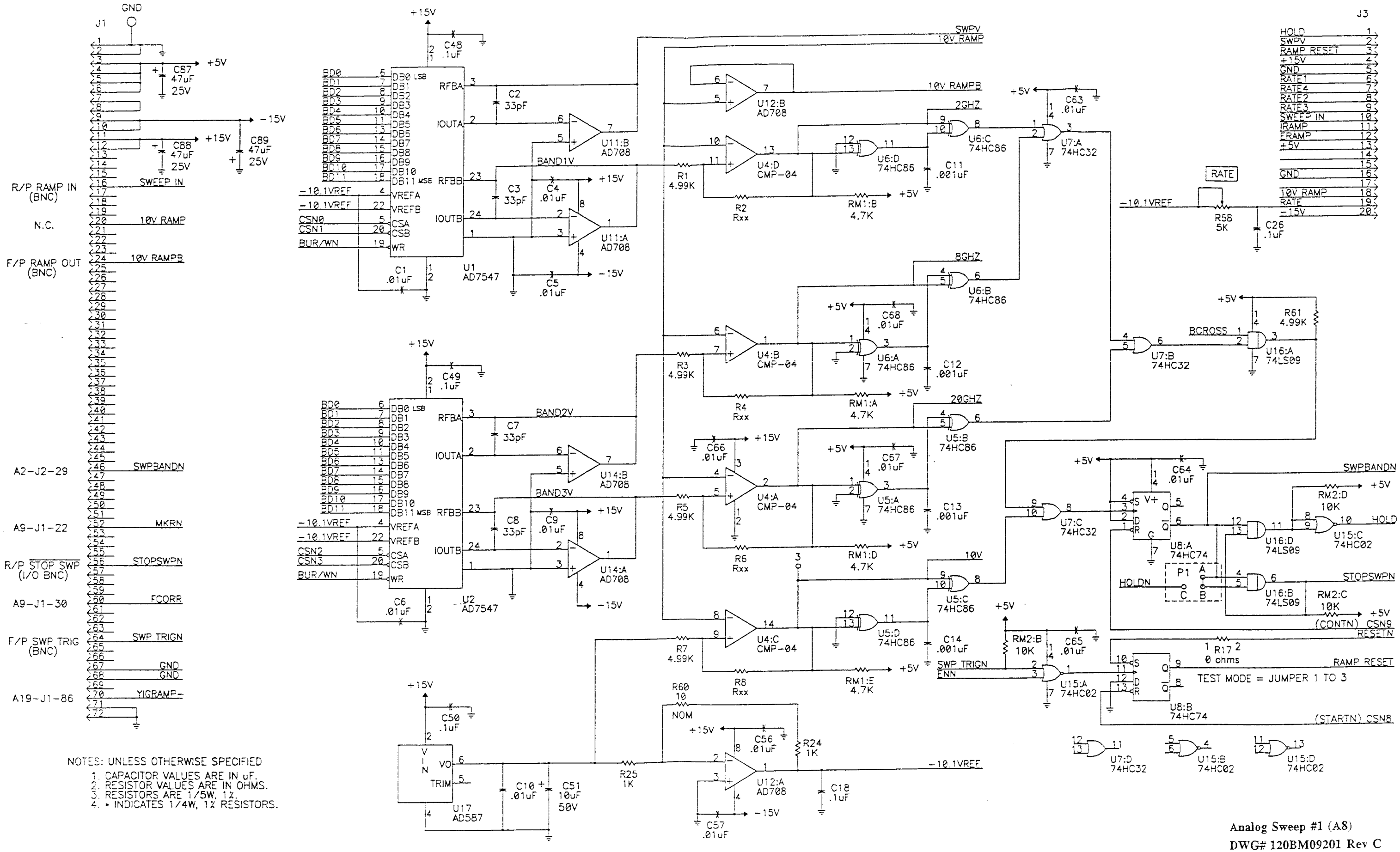
The DAC U1 section A gives a DC voltage at the output of U11 B which determines the rate at which the unit sweeps. DACs U1 B, U2 A and B are set up to give a voltage at the output of their respective amp (U11 A, U14 B and A) which corresponds to frequency band changes. Namely at 2, 8 and 20 GHz. Specifically, for the 2 GHz band switch point the voltage from U11-1 is the reference voltage for comparator U4 D. The 10V_RAMP from A8A1 is the other input to the comparator. When the ramp voltage reaches the reference voltage the comparator switches resulting in a pulse at U6-8 which propagates thru U7 clocking flip flop U8 A. This causes the Q output to go low signaling the computer that a band change must take place. This Q output also causes the hold line (U15-10) to trigger thereby stopping the ramp on the A8A1 board. In addition the signal is output to the rear panel as the STOP SWP I/O logic signal. When the band change is complete the computer sends a signal CONTN to reset the flip flop U8. The 8 and 20 GHz band changes work similarly.

The 10 volt reference from U17 is inverted by U12 giving a negative reference. The +10V reference is used as the reference for U4 C comparator. This comparator switches at the end of each sweep and generates a pulse. When the SWP_TRIGN signal is received, (this signal is a result of the front panel SWP TRIG input) U15 A and U8 B cause the RAMP_RESET line to reset the ramp voltage on A8A1.

The 10V_RAMP is applied to U19 A where it is inverted and then summed at U19 B with different offset voltages, switched by U18, at each band change. These offset voltages cause the ramp at U19-7 to start at 0V for each new band. The amplitude of the ramps are then adjusted by DAC U20 section A and B (using both sections gives a greater range). The resulting ramp is buffered by U47 B and summed together at U22 B with other signals, including the frequency correction signal from the digital ramp board A9. The switch U23 can then select the ramp or an inverted version of this ramp (U22 A) for output to the YIG driver depending on whether the frequency sweep is increasing or decreasing. Another signal is summed into the ramp at U22 B this signal is YIG lag compensation. At the start of each band U16 C triggers U24 A causing a pulse at the Q not output. The negative going pulse at U25 A is turned into a negative going spike with decay by the diode CR3 and C20. This is buffered by U25 B and its amplitude is adjusted by DAC U46 according to the sweep rate. The amplitude of the spike is maximum for the highest sweep rate. The output of U47 A is then summed with the frequency correction and the ramp voltage at U22 B.

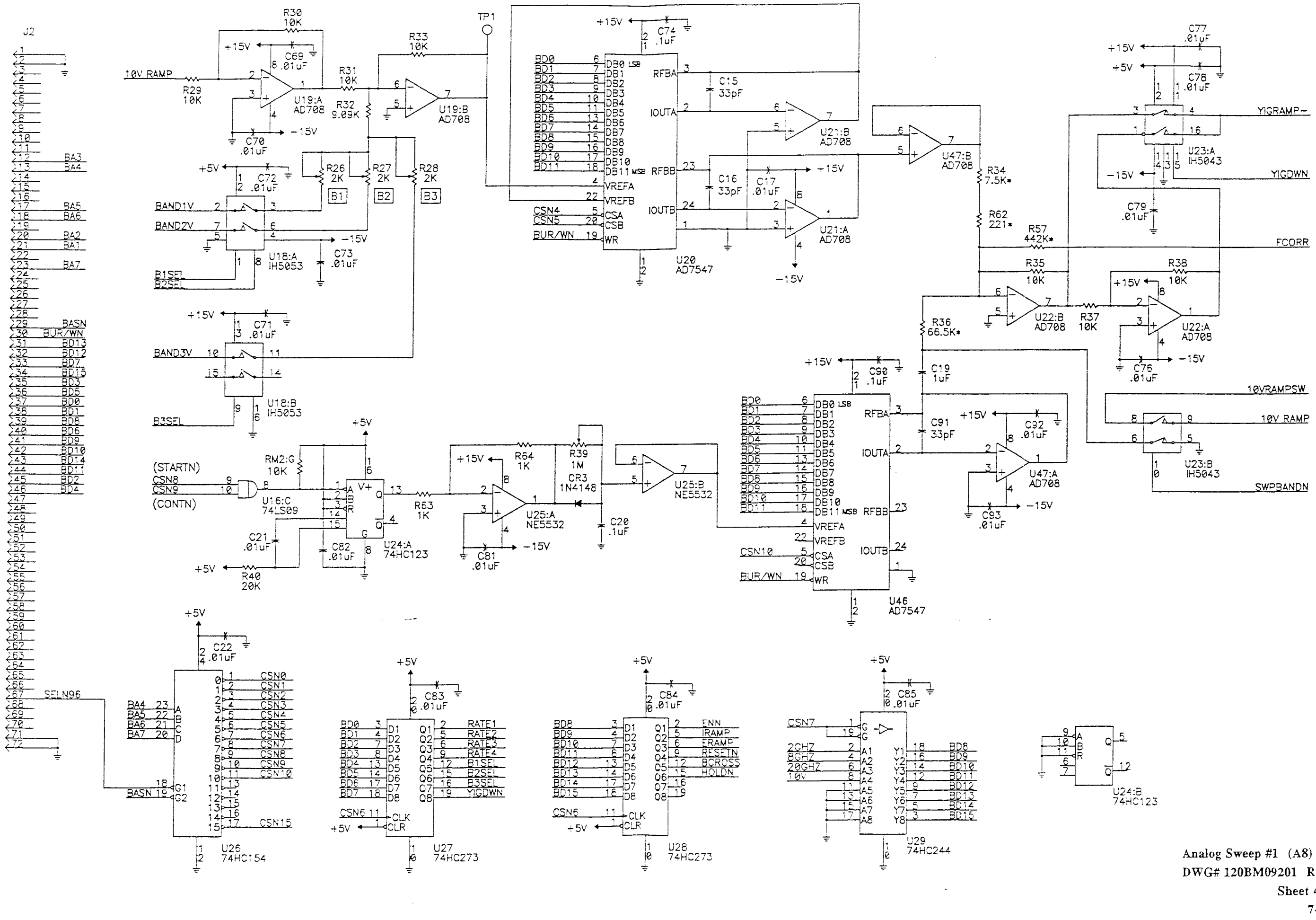
U32 thru U35 DACs provide reference voltages for up to 8 analog sweep markers. For example, when a marker is set DAC U32 A generates a reference voltage at U36-7 for comparators U40 C and D. When the 10V_RAMP reaches the reference voltage the comparators flip generating a marker pulse at the output U40 pin 13 and 14. The width of this pulse is determined by IR1 and R41. The pulse then propagates thru U45 and is buffered to be supplied to the rear panel. The rest of the markers are generated in the same way and are NOR'ed together at U45.

U44 and U26 decode chip selects for the board. U27, U28 and U29 provide buffering necessary for computer bus interface.

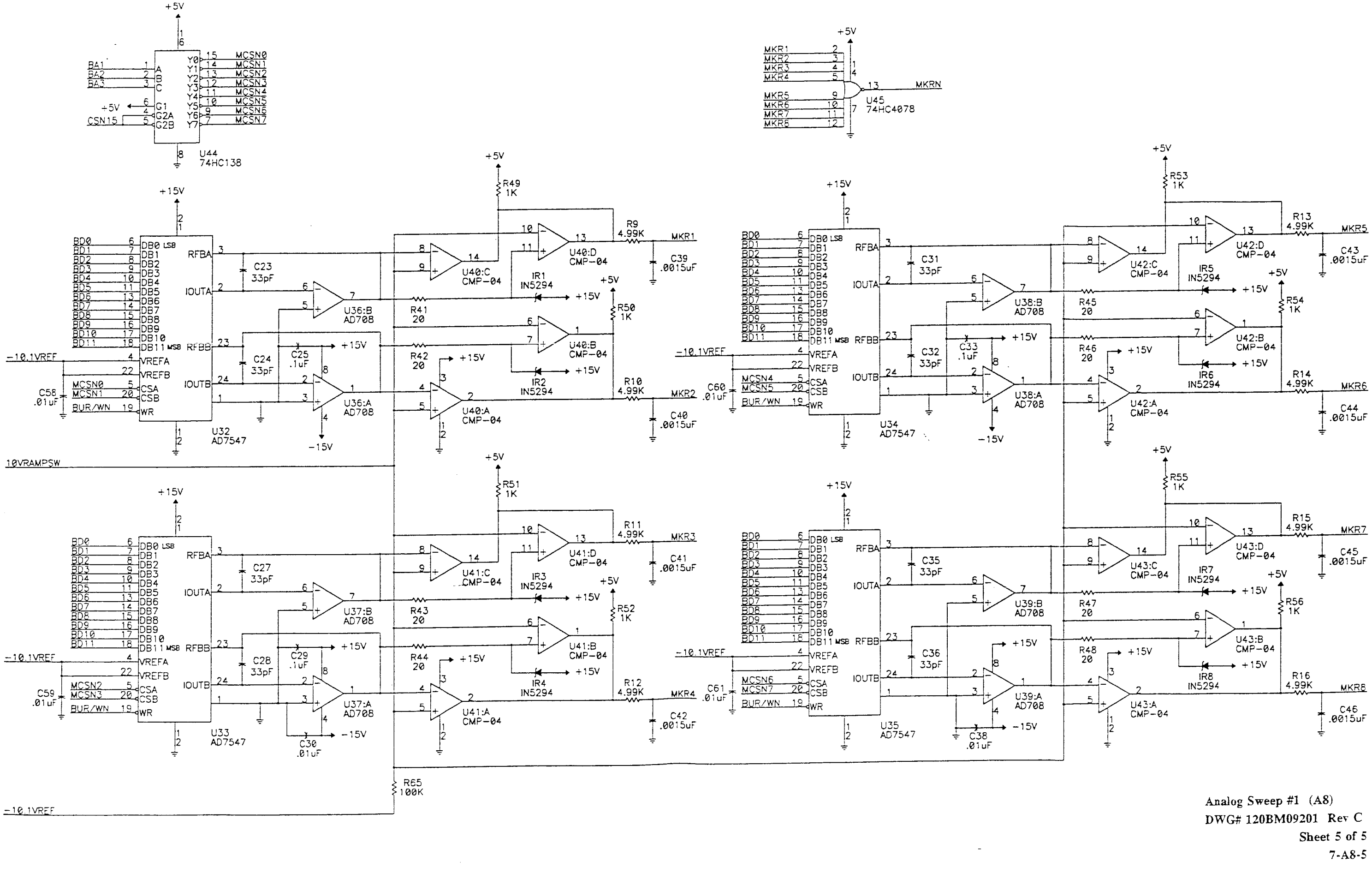


NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITOR VALUES ARE IN uF.
2. RESISTOR VALUES ARE IN OHMS.
3. RESISTORS ARE 1/5W, 1%.
4. • INDICATES 1/4W, 1% RESISTORS.

Analog Sweep #1 (A8)
DWG# 120BM09201 Rev C
Sheet 3 of 5
7-A8-3



Analog Sweep #1 (A8)
DWG# 120BM09201 Rev C
Sheet 4 of 5
7-A8-4



Analog Sweep #1 (A8)
DWG# 120BM09201 Rev C
Sheet 5 of 5
7-A8-5

8 Options

The following options are available for Model 7200, and are discussed under separate headings:

Option 11: External 5 MHz Time Base

Option 16: *(See note below)*

Option 17: Fast Scan Modulation

Option 22: Rear Panel RF Output Connector

Option 24: Internal Modulation

Option 25: Planar Crown Connector

Option 28: High Stability Timebase

NOTE:

1 Hz resolution, which is Option 16 in other Giga-tronics instruments, is a standard feature of Model 7200. Circuits and components associated with this feature are sometimes (as in parts lists) referred to as being part of Option 16, but in the case of this model they are considered standard.

8.1 OPTION 11: 5 MHz EXTERNAL TIME BASE

This option makes it possible to use an external 5 MHz time base, in addition to the standard 10 MHz internal or external time base. The option requires installation of the A115 PC board (the parts list and drawings for this circuit are incorporated in sections 6 and 7 of the manual)

The 5 MHz input should be applied to the rear panel 'REF IN' BNC connector.

To specify the frequency of the external time base, press **[SHIFT] [SPECIAL] [11]**. Press **[MODE]** to toggle the entry menu display between the 5 MHz and 10 MHz settings.

The default setting is 5 MHz for instruments with Option 11.

8.2 OPTION 17: FAST SCAN MODULATION

In instruments with Option 17, the scan modulator (a PIN diode attenuator) is inserted between the level control system and the output step attenuator. This modulator is digitally controlled and linearized, and can operate in Scan mode (DC coupled) or AM mode (AC coupled). The AM mode of scan modulation is referred to as 'Fast AM' to distinguish it from the instrument's standard amplitude modulation feature. Fast AM can be operated simultaneously with pulse modulation.

8.2.1 SPECIFICATIONS: DC Coupled ('SCAN') Mode

DYNAMIC RANGE:	40 dB, minimum
LINEARITY (at cal points):	± 0.6 dB (0 to 20 dB), ± 1 dB (20 to 50 dB). Standard calibration points are at 1, 4, 8, 12, 14, 16, 18, and 20 GHz.
FREQUENCY RESPONSE:	DC to 150 kHz, sine wave
RISE/FALL TIME RESPONSE TO STEP INPUT:	0.5 µs up to 40 dB step
DELAY TIME:	0.5 µs, typical
SENSITIVITY:	0.1 V/dB (10 dB/V)
INPUT IMPEDANCE:	50 Ω, nominal

8.2.2 SPECIFICATIONS: AC Coupled ('AM' Mode)

MODULATION DEPTH:	0 to 90%
RF OUTPUT LEVEL:	approx. 11 dB below generator setting
FREQUENCY RESPONSE:	10 Hz to 50 kHz
TOTAL HARMONIC DISTORTION:	5% max. (2% typical) at 80% modulation; 10% max. (5% typical) at 30% modulation
INPUT SENSITIVITY:	1 Vpp, for 50% modulation at 1 kHz
INPUT IMPEDANCE:	50 Ω, nominal
INSERTION LOSS:	5 dB max. (3 dB typical); bypassed when not in use

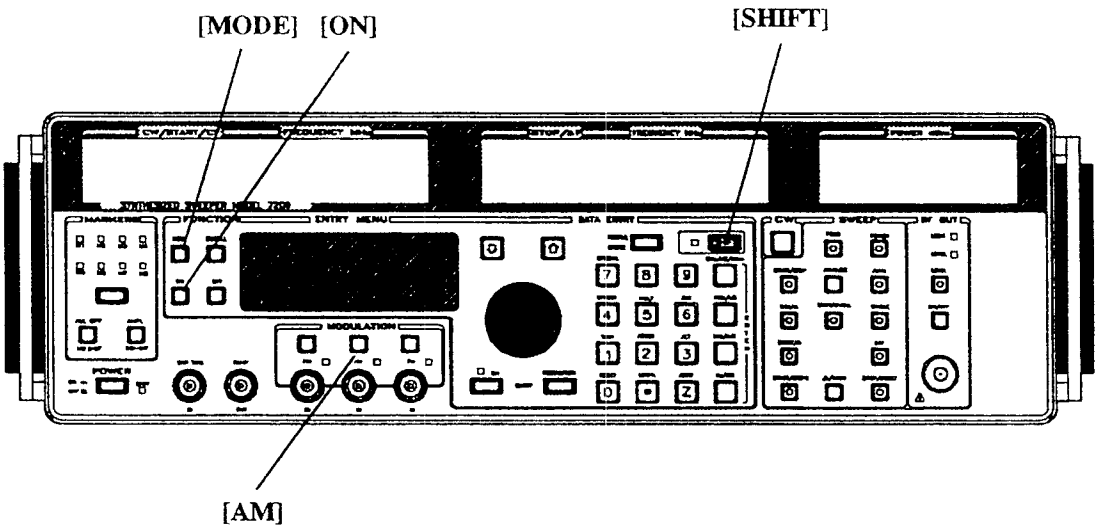


Figure 8.1: Option 17 modes

8.2.3 Option 17 Front Panel Operation

To select either of the modulation modes provided under Option 17, press **[SHIFT]** [AM]. The entry menu display should read 'SCAN EXT: OFF'. This indicates that Scan mode is selected but is presently turned off; use the **[ON]** button to activate this mode. Scan modulation requires an external input, which must be supplied to the 'SCAN' input BNC connector on the rear panel.

To select any of the Fast AM modes, press the **[MODE]** button. The choices are:

AMfSIN = Fast AM, sine wave

AMfSQR = Fast AM, square wave

AMfTRI = Fast AM, triangle wave

AMfEXT = Fast AM, external wave

All Fast AM modes function in the same way as the standard AM modes described in Section 2 of the manual, except that, in the case of external modulation, the modulation input is supplied to the rear panel 'SCAN' connector.

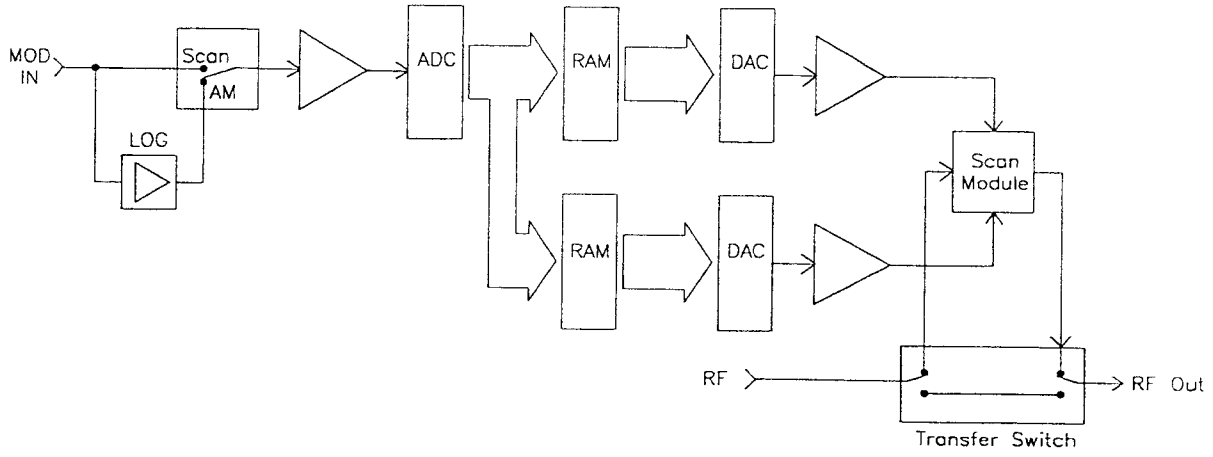


Figure 8.2: Fast scan modulation

8.2.4 Option 17 Theory of Operation

The modulating waveform (internally or externally generated) is sent through either of two input paths. If Fast AM mode, rather than Scan mode, is activated, the modulation signal passes through a logarithmic amplifier followed by a DC amplifier; if the Scan mode is activated, the modulation signal bypasses the log amp and passes through the DC amp only.

The output of the DC amplifier is converted to digital values by a pair of analog-to-digital converters. The digital values are applied to the address lines of a pair of RAMs. The RAMs hold characterization and linearization data for the scan modulator; as the input waveform changes, different areas of memory are addressed, so that the correction factors stored in memory are constantly tracking the input.

The correction data read from the RAMs is applied to a pair of digital-to-analog converters; the outputs of these DACs drive a pair of DC amplifiers, which in turn provide the positive and negative current sources to the scan modulator.

A transfer switch is used to switch the scan modulator into and out of the RF output path, so that it does not cause power loss when scan modulation is not in use.

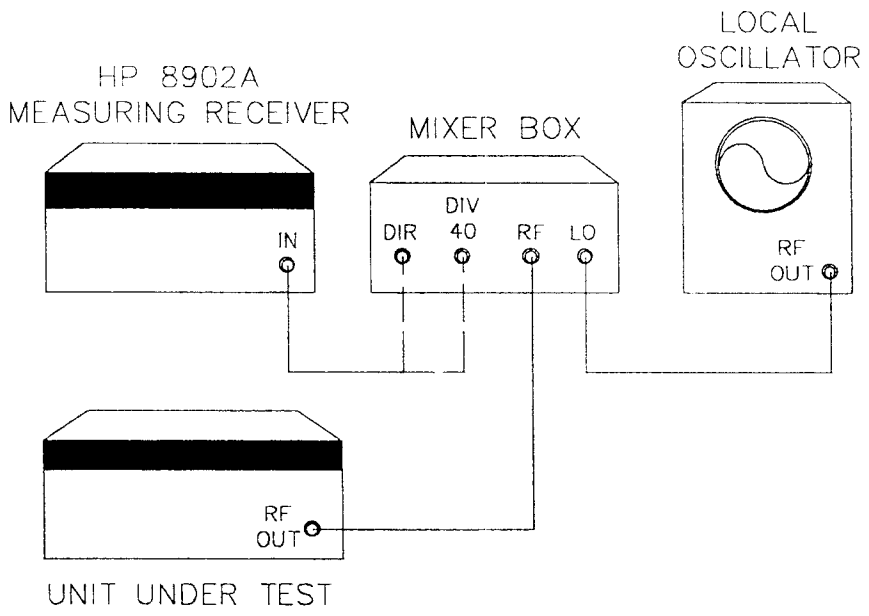


Figure 8.3: Scan test setup

8.2.5 Option 17 Acceptance Test Procedure (Fast AM Mode)

1. Select 'AMf EXT: ON'.
2. Connect the Model 7200 RF output to a mixer box, as shown in the illustration. On the 8902, select 50 Hz and 15 kHz filters, AM mode. Set the 7200 RF output frequency to 5 GHz. Using a BNC 'T' connector and oscilloscope, apply a 1.0 Vpp, 1 kHz sine wave to the 'SCAN' input BNC on the Series 7200 rear panel.
3. Measure the percentage of distortion at 1 kHz; verify that distortion is ≤5%.
4. Increase the input modulation to obtain 80% AM. Verify that distortion is <5%.
5. Check the distortion at 30% and 80% modulation at the following frequencies: 1 GHz, 5 GHz, 15 GHz, and 22 GHz.
6. Disconnect external modulation. Select 'AMfSIN: ON', 1 kHz rate, 50% depth. Using 8902A, measure AM%. Verify a modulation reading of 47 to 53%. Verify a distortion reading of <5% at 1 kHz.
7. Select 'AMfSQR: ON', 50% depth. Turn off all filters on 8902A. Verify an AM% reading of 45 to 55% on 8902A.
8. Select 'AMfTRI: ON', 50% depth. Turn on 50 Hz and 15 kHz filters on 8902A. Verify an AM% reading of 47 to 53% on 8902A.
9. Connect a detector to Series 7200 RF out. Connect detector output to scope, channel B, 50 Ω on. Set scope to 2 mV and 200 µs.
10. Select 'AMfEXT: ON'.
11. Apply a 1 Vpp, 1 kHz sine wave to the 'SCAN' input BNC. Adjust the channel B input vernier for a display of the waveform that spans six vertical divisions.
12. Adjust the external modulation rate for 10 Hz; verify that the displayed waveform has an amplitude of >4 divisions on the scope. Vary the rate from 10 Hz to 100 kHz, and verify that the waveform amplitude maintains an amplitude of ≥4 divisions.

8.2.6 Option 17 Acceptance Test Procedure (Scan Mode)

1. Apply a 0-1 V (10 dB depth) sine wave to the 'SCAN' input BNC.
2. Select 'SCAN EXT: ON'.
3. Connect a detector to the Model 7200 RF output, and connect the output of the detector to the oscilloscope (channel B, 50 Ω on). Set oscilloscope to 2mV, 200 µs, and adjust the channel B input vernier for a display of the waveform that spans six vertical divisions.
4. Vary the external modulation rate between 1 kHz and 300 kHz; verify that the displayed waveform maintains a minimum amplitude of 4 vertical divisions.
5. Set the modulation rate to 50 kHz, square wave. Compare the input modulation rising edge with the detector output rising edge; verify that the delay is less than 800 ns.
6. Compare the input modulation falling edge with the detector output falling edge; verify that the delay is approximately 1 µs.
7. Connect the Model 7200 RF output to the spectrum analyzer. Set the RF output frequency to 1 GHz. Set the analyzer span to 5 MHz and center the 1 GHz signal on the screen. Set the span to 0 Hz. Apply a 0-4V sine wave to the 'SCAN' input BNC. Verify a 0 to -40 dB sine wave on the analyzer. Change the input sine wave to 0-2V; verify a 0 to -20 dB sine wave on the analyzer. Change the input sine wave to a triangle wave and square wave; verify clean waveforms on the analyzer screen from 0 to -20 dB.

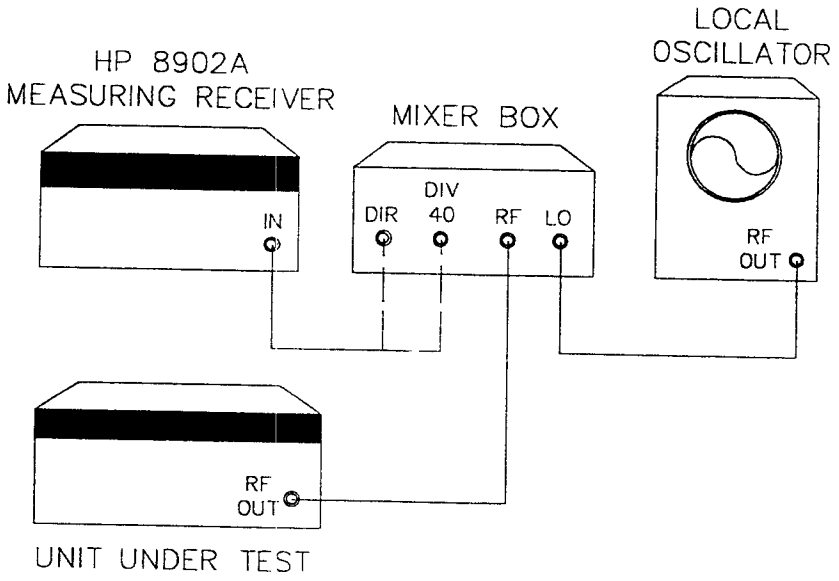


Figure 8.4: Scan calibration setup

8.2.7 Option 17 Calibration

1. Select 'AMfEXT: ON', but do not apply a modulating signal.
2. Measure TP3 on the Scan Modulation PC board (A7), and verify a DVM reading of +2.5 V, ±.05 V.
3. Move the jumper on P1-1 and P1-6 to P1-2 and P1-5.
4. Adjust the Zero pot (R14) for a DVM reading of 0.0 VDC on TP1.
5. Move the jumper on P1-2 and P1-5 to P1-3 and P1-4.
6. Adjust the Gain pot (R19) for a DVM reading of +6.0 VDC on TP1.
7. Move the jumper on P1-3 and P1-4 to P1-1 and P1-6.

8. Adjust the Level pot (R25) for a DVM reading of +0.65 VDC on TP1.
9. Connect the Model 7200 and test equipment as shown in the illustration. On the 8902, select 50 Hz and 15 kHz filers, AM mode. Set the 7200 RF output to 5 GHz.
10. Using a BNC 'T' connector and oscilloscope, apply a 1.0 Vpp, 1 kHz sine wave to the 'SCAN' input BNC on the Model 7200 rear panel.
11. Adjust the Sense pot (R4) for a 50.0% reading on the 8902.
12. Measure the distortion at 1 kHz; adjust the Gain pot (R19) for the lowest distortion reading.

Check the distortion at the RF output frequencies shown in the following table. Adjust R19 as needed to bring the distortion within the acceptable range at all calibration points.

FAST AM CALIBRATION POINTS		
RF Frequency	**Distortion at 80%**	**Distortion at 30%**
1 GHz	<5%	<10%
5 GHz	<5%	<10%
15 GHz	<5%	<10%
22 GHz	<5%	<10%

Select 'AMfSQR: ON', depth 50%. Turn off all filters on 8902A, and verify an AM% reading of 45-55% on the 8902A.

Select 'AMfTRI: ON', depth 50%. Turn on 50 Hz and 15 kHz filters on the 8902A, and verify an AM% reading of 47-53% on 8902A.

8.2.8 Option 17 Assemblies

The parts lists and drawings for assemblies that are required for Option 17 are incorporated into the manual. See page 6-25 for a list of these assemblies.

8.3 OPTION 22: REAR PANEL RF OUTPUT CONNECTOR

If Option 22 is installed, the RF output connector is relocated to the rear panel of the Model 7200. This option may reduce RF output power by as much as 2 dB.

The components required by Option 22 are listed on page 6-26.

8.4 OPTION 24: INTERNAL MODULATION

This option provides a built-in pulse generator and two built-in function generators for creating PM, AM, and FM envelopes.

This option has been incorporated into the main body of the manual; procedures and specifications which apply only to instruments with Option 24 are so noted. The assemblies required by Option 24 are listed on page 6-26.

8.5 OPTION 25: PLANAR CROWN RF OUTPUT CONNECTOR

If Option 25 is installed, the RF output connector is replaced by a Planar Crown Universal Connector, manufactured by Lucas Weinschel. This is a two-part connector; the components are referred to as the planar bulkhead and the planar crown. The bulkhead is a 2.9 mm female connector, mounted inward of the front panel, which is common to all implementations of Option 25 (see the Option 25 parts list on page 6-26). The crown is attached to the bulkhead on the outward side of the front panel, and is available in a variety of versions, as shown in the table below:

Giga-tronics Part#	Weinschel Part#	Connector Type	Frequency Range (GHz)
JRWC-00030	7005-3	type N female crown	DC to 18
JRWC-00040	7005A-4	type N male crown	DC to 18
JRWC-00050	7005A-5	type GPC-7 crown	DC to 18
JRWC-00080	7005A-8	type TNC female crown	DC to 18
JRWC-00090	7005A-09	type TNC male crown	DC to 18
JRWC-00010	7005A-1	type SMA female crown	DC to 26.5
JRWC-00020	7005A-2	type SMA male crown	DC to 26.5
JRWC-00060	7005A-6	3.5 mm female crown	DC to 34
JRWC-00070	7005A-7	3.5 mm male crown	DC to 34
JRWC-00100	7005A-10	2.92 mm female crown	DC to 40
JRWC-00110	7005A-11	2.92 mm male crown	DC to 40

8.6 OPTION 28: HIGH STABILITY TIMEBASE

If Option 28 is intalled, the standard 10 MHz timebase oscillator (see PC board A21) is replaced by one having an aging rate specification of 5×10^{-10}/day.

9 Special Configurations

9.1 SPECIAL CONFIGURATIONS

If the instrument is specially configured (as indicated by a three-digit number on the "Config." line of the Model/Serial/Config. sticker), a supplement describing the configuration is added to the manual, beginning on the following page. Modifications of the instrument, its circuits, and its performance characteristics are listed in that supplement.

Manual Changes Supplement
November 21, 1995

This supplement lists any manual errors which were discovered after printing (these are placed under the heading 'Errata'), together with any revisions of circuits or assemblies which were implemented after printing (these are placed under the heading 'Design Changes').

Design Changes, p. 2 of 2

The Output PLL PC board (A18) may be changed to Revision C. The circuit is modified as follows: R64 is changed to 5.62K, nominal. R70 is changed to 6.98K, nominal. L6 is changed to 470 µH. L7 is replaced by a jumper (Item 3, Part# WSTB-269XX).

The Pulse Generator PC board (A5A1) may be changed to Revision D. This change affects the method of assembly only, and does not modify the circuit as it is described in the manual.

The Function Generator PC board (A6A1) may be changed to Revision C. This change affects the method of assembly only, and does not modify the circuit as it is described in the manual.

The Memory PC board (A3) may be changed to Revision D. This change corrects the parts list and the assembly drawing, which had omitted PROMs U5 and U6 (part #UMN0-27256). U5 is placed between U3 and U7; U6 is placed between U4 and U8.

Parts List for 120BA09201 ANALOG SWEEP #1 PCA Rev C

Item	Part Number	Qty	CAGE	Mfr's Part Number	Description
0	120BS09201	Ref	58900	120BS09201	ANALOG SWEEP #1 SCH
1	120CF09210	1	58900	120CF09210	ANALOG SWEEP 1 PCB
2	ETST-06224	2	88245	1280B	TURRET TERMINAL
3	JJF0-02000	1		89F4578	TWO CONTACT JUMPER
101	HBPP-44005	1	96906	MS-51957-14	4-40 X 5/16 PAN
102	HWFS-40400	1	96906	MS15795-803	#4 X 1/4 FLAT WASHER
103	HWSS-40300	1	96906	MS35338-135	#4 X 3/16 SPLIT LOCK
A8 A1	120BA11401	1	58900	120BA11401	ANALOG SWEEP #2 PCA
C 1	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 2	CC50-00330	1	52763	EDPT-33-NP0-5%	33 PF CERAMIC NP0
C 3	CC50-00330	1	52763	EDPT-33-NP0-5%	33 PF CERAMIC NP0
C 4	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 5	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 6	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 7	CC50-00330	1	52763	EDPT-33-NP0-5%	33 PF CERAMIC NP0
C 8	CC50-00330	1	52763	EDPT-33-NP0-5%	33 PF CERAMIC NP0
C 9	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 10	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 11	CC50-02100	1	52763	EDPT-1000-Y5P10%	.001 UF CERAMIC Y5P
C 12	CC50-02100	1	52763	EDPT-1000-Y5P10%	.001 UF CERAMIC Y5P
C 13	CC50-02100	1	52763	EDPT-1000-Y5P10%	.001 UF CERAMIC Y5P
C 14	CC50-02100	1	52763	EDPT-1000-Y5P10%	.001 UF CERAMIC Y5P
C 15	CC50-00330	1	52763	EDPT-33-NP0-5%	33 PF CERAMIC NP0
C 16	CC50-00330	1	52763	EDPT-33-NP0-5%	33 PF CERAMIC NP0
C 17	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 18	CC50-04100	1	56289	1C20Z5U104M050B	.1 UF CERAMIC Z5U
C 19	CC50-05100	1	56289	2C2525U105M050B	1 UF CERAMIC Z5U
C 20	CC50-04100	1	56289	1C20Z5U104M050B	.1 UF CERAMIC Z5U
C 21	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 22	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 23	CC50-00330	1	52763	EDPT-33-NP0-5%	33 PF CERAMIC NP0
C 24	CC50-00330	1	52763	EDPT-33-NP0-5%	33 PF CERAMIC NP0
C 25	CC50-04100	1	56289	1C20Z5U104M050B	.1 UF CERAMIC Z5U
C 26	CC50-04100	1	56289	1C20Z5U104M050B	.1 UF CERAMIC Z5U
C 27	CC50-00330	1	52763	EDPT-33-NP0-5%	33 PF CERAMIC NP0
C 28	CC50-00330	1	52763	EDPT-33-NP0-5%	33 PF CERAMIC NP0
C 29	CC50-04100	1	56289	1C20Z5U104M050B	.1 UF CERAMIC Z5U
C 30	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 31	CC50-00330	1	52763	EDPT-33-NP0-5%	33 PF CERAMIC NP0
C 32	CC50-00330	1	52763	EDPT-33-NP0-5%	33 PF CERAMIC NP0
C 33	CC50-04100	1	56289	1C20Z5U104M050B	.1 UF CERAMIC Z5U
C 35	CC50-00330	1	52763	EDPT-33-NP0-5%	33 PF CERAMIC NP0
C 36	CC50-00330	1	52763	EDPT-33-NP0-5%	33 PF CERAMIC NP0
C 38	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 39	CC50-02150	1	51642	200-050-NP0-152J	1500 PF CERAMIC
C 40	CC50-02150	1	51642	200-050-NP0-152J	1500 PF CERAMIC
C 41	CC50-02150	1	51642	200-050-NP0-152J	1500 PF CERAMIC
C 42	CC50-02150	1	51642	200-050-NP0-152J	1500 PF CERAMIC
C 43	CC50-02150	1	51642	200-050-NP0-152J	1500 PF CERAMIC
C 44	CC50-02150	1	51642	200-050-NP0-152J	1500 PF CERAMIC
C 45	CC50-02150	1	51642	200-050-NP0-152J	1500 PF CERAMIC
C 46	CC50-02150	1	51642	200-050-NP0-152J	1500 PF CERAMIC
C 48	CC50-04100	1	56289	1C20Z5U104M050B	.1 UF CERAMIC Z5U
C 49	CC50-04100	1	56289	1C20Z5U104M050B	.1 UF CERAMIC Z5U

Parts List for 120BA09201 ANALOG SWEEP #1 PCA Rev C

Item	Part Number	Qty	CAGE	Mfr's Part Number	Description
C 50	CC50-04100	1	56289	1C20Z5U104M050B	.1 UF CERAMIC Z5U
C 51	CE50-R6100	1	2M734	ECEAIHU100	10 UF 50V RADIAL LEAD
C 56	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 57	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 58	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 59	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 60	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 61	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 63	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 64	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 65	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 66	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 67	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 68	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 69	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 70	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 71	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 72	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 73	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 74	CC50-04100	1	56289	1C20Z5U104M050B	.1 UF CERAMIC Z5U
C 76	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 77	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 78	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 79	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 81	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 82	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 83	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 84	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 85	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 87	CE25-R6470	1	16508	ECEA1EU470	47 UF 25V RADIAL LEAD
C 88	CE25-R6470	1	16508	ECEA1EU470	47 UF 25V RADIAL LEAD
C 89	CE25-R6470	1	16508	ECEA1EU470	47 UF 25V RADIAL LEAD
C 90	CC50-04100	1	56289	1C20Z5U104M050B	.1 UF CERAMIC Z5U
C 91	CC50-00330	1	52763	EDPT-33-NPO-5%	33 PF CERAMIC NPO
C 92	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
C 93	CC50-03100	1	51642	150-100-W5R-103K	.01 UF CERAMIC X7R
CR 3	DSA0-04148	1	07263	1N4148	IN4148 G.P. DIODE
IR 1	DZAC-05294	1	04713	IN5294	IN5294 .75mA REG DIODE
IR 2	DZAC-05294	1	04713	IN5294	IN5294 .75mA REG DIODE
IR 3	DZAC-05294	1	04713	IN5294	IN5294 .75mA REG DIODE
IR 4	DZAC-05294	1	04713	IN5294	IN5294 .75mA REG DIODE
IR 5	DZAC-05294	1	04713	IN5294	IN5294 .75mA REG DIODE
IR 6	DZAC-05294	1	04713	IN5294	IN5294 .75mA REG DIODE
IR 7	DZAC-05294	1	04713	IN5294	IN5294 .75mA REG DIODE
IR 8	DZAC-05294	1	04713	IN5294	IN5294 .75mA REG DIODE
J 3	JIB2-20170	1	55322	SLW-110-01-S-D	20 PIN STRIPLINE SOCKET
P 1	JIA1-03230	1	52072	CA-503-23B-43	3 PIN STRIPLINE PLUG
R 1	RN50-14990	1	65940	CRB20FX4991	4.99K;M F;1/5W;1%;100PPM
R 3	RN50-14990	1	65940	CRB20FX4991	4.99K;M F;1/5W;1%;100PPM
R 5	RN50-14990	1	65940	CRB20FX4991	4.99K;M F;1/5W;1%;100PPM
R 7	RN50-14990	1	65940	CRB20FX4991	4.99K;M F;1/5W;1%;100PPM
R 9	RN50-14990	1	65940	CRB20FX4991	4.99K;M F;1/5W;1%;100PPM
R 10	RN50-14990	1	65940	CRB20FX4991	4.99K;M F;1/5W;1%;100PPM
R 11	RN50-14990	1	65940	CRB20FX4991	4.99K;M F;1/5W;1%;100PPM

Parts List for 120BA09201 ANALOG SWEEP #1 PCA Rev C

Item	Part Number	Qty	CAGE	Mfr's Part Number	Description
R 12	RN50-14990	1	65940	CRB20FX4991	4.99K;M F;1/5W;1%;100PPM
R 13	RN50-14990	1	65940	CRB20FX4991	4.99K;M F;1/5W;1%;100PPM
R 14	RN50-14990	1	65940	CRB20FX4991	4.99K;M F;1/5W;1%;100PPM
R 15	RN50-14990	1	65940	CRB20FX4991	4.99K;M F;1/5W;1%;100PPM
R 16	RN50-14990	1	65940	CRB20FX4991	4.99K;M F;1/5W;1%;100PPM
R 17	WJIB-02022	1	53387	923345-02	.2" INSULATED JUMPER
R 24	RN50-11000	1	81349	RN50C1001F	1.00 K OHMS 1% MET FILM
R 25	RN50-11000	1	81349	RN50C1001F	1.00 K OHMS 1% MET FILM
R 26	RAPG-12000	1	32997	3296Z-1-202	2K 10% 25T .5W POT.
R 27	RAPG-12000	1	32997	3296Z-1-202	2K 10% 25T .5W POT.
R 28	RAPG-12000	1	32997	3296Z-1-202	2K 10% 25T .5W POT.
R 29	RN50-21000	1	65940	CRB20FX1002	10.0K;M F;1/5W;1%;100PPM
R 30	RN50-21000	1	65940	CRB20FX1002	10.0K;M F;1/5W;1%;100PPM
R 31	RN50-21000	1	65940	CRB20FX1002	10.0K;M F;1/5W;1%;100PPM
R 32	RN50-19090	1	65940	CRB20FX9091	9.09K;M F;1/5W;1%;100PPM
R 33	RN50-21000	1	65940	CRB20FX1002	10.0K;M F;1/5W;1%;100PPM
R 34	RN55-17500	1	81349	RN55D7501F	7.5 K OHMS 1% MET FILM
R 35	RN50-21000	1	65940	CRB20FX1002	10.0K;M F;1/5W;1%;100PPM
R 36	RN55-26650	1	81349	RN55D6652F	66.5 K OHMS 1% MET FILM
R 37	RN50-21000	1	65940	CRB20FX1002	10.0K;M F;1/5W;1%;100PPM
R 38	RN50-21000	1	65940	CRB20FX1002	10.0K;M F;1/5W;1%;100PPM
R 39	RAPG-41000	1	32997	3296Z-1-105	1M 10% 25T .5W TRIM. POT
R 40	RN50-22000	1	65940	CRB20FX2002	20.0K;M F;1/5W;1%;100PPM
R 41	RN50-00200	1	65940	CRB20FX20R0	20.0;M F;1/5W;1%;100PPM
R 42	RN50-00200	1	65940	CRB20FX20R0	20.0;M F;1/5W;1%;100PPM
R 43	RN50-00200	1	65940	CRB20FX20R0	20.0;M F;1/5W;1%;100PPM
R 44	RN50-00200	1	65940	CRB20FX20R0	20.0;M F;1/5W;1%;100PPM
R 45	RN50-00200	1	65940	CRB20FX20R0	20.0;M F;1/5W;1%;100PPM
R 46	RN50-00200	1	65940	CRB20FX20R0	20.0;M F;1/5W;1%;100PPM
R 47	RN50-00200	1	65940	CRB20FX20R0	20.0;M F;1/5W;1%;100PPM
R 48	RN50-00200	1	65940	CRB20FX20R0	20.0;M F;1/5W;1%;100PPM
R 49	RN50-11000	1	81349	RN50C1001F	1.00 K OHMS 1% MET FILM
R 50	RN50-11000	1	81349	RN50C1001F	1.00 K OHMS 1% MET FILM
R 51	RN50-11000	1	81349	RN50C1001F	1.00 K OHMS 1% MET FILM
R 52	RN50-11000	1	81349	RN50C1001F	1.00 K OHMS 1% MET FILM
R 53	RN50-11000	1	81349	RN50C1001F	1.00 K OHMS 1% MET FILM
R 54	RN50-11000	1	81349	RN50C1001F	1.00 K OHMS 1% MET FILM
R 55	RN50-11000	1	81349	RN50C1001F	1.00 K OHMS 1% MET FILM
R 56	RN50-11000	1	81349	RN50C1001F	1.00 K OHMS 1% MET FILM
R 57	RN55-34420	1	81349	RN55D4423F	442 K OHMS 1% MET FILM
R 58	RAPG-15000	1	32997	3296Z-1-502	5K 10% 25T .5W TRIM. POT
R 60	RN50-00100	1	65940	CRB20FX10R0	10.0;M F;1/5W;1%;100PPM
R 61	RN50-14990	1	65940	CRB20FX4991	4.99K;M F;1/5W;1%;100PPM
R 62	RN55-02210	1	81349	RN55D2210F	221 OHMS 1% MET FILM
R 63	RN50-11000	1	81349	RN50C1001F	1.00 K OHMS 1% MET FILM
R 64	RN50-11000	1	81349	RN50C1001F	1.00 K OHMS 1% MET FILM
R 65	RN50-31000	1	65940	CRB20FX1003	100K;M F;1/5W;1%;100PPM
RM 1	RM5S-14700	1	71450	750-61-R4.7K	5 X 4.7K SIP RESISTOR NE
RM 2	RM7S-21000	1	71450	750-81-R10K	10K OHM X 7 SIP NETWRK
RX 2	RN50-?????	Ref	65940	CRB20FX????	SELECTED IN TEST
RX 4	RN50-?????	Ref	65940	CRB20FX????	SELECTED IN TEST
RX 6	RN50-?????	Ref	65940	CRB20FX????	SELECTED IN TEST
RX 8	RN50-?????	Ref	65940	CRB20FX????	SELECTED IN TEST
U 1	UIN0-07547	1	24355	AD7547KN	AD7547KN;DUAL 12 BIT DAC

Parts List for 120BA09201 ANALOG SWEEP #1 PCA Rev C

	Item	Part Number	Qty	CAGE	Mfr's Part Number	Description
U	2	UIN0-07547	1	24355	AD7547KN	AD7547KN;DUAL 12 BIT DAC
U	4	ULN0-00004	1	PMI	CMP04FP	CMP04;QUAD COMPARATOR
U	5	UTN0-00862	1	01295	74HC86N	QUAD 2 INPUT X OR GATE
U	6	UTN0-00862	1	01295	74HC86N	QUAD 2 INPUT X OR GATE
U	7	UTN0-00322	1	18714	74HC32E	QUAD 2 INPUT OR GATE
U	8	UTN0-00742	1	18714	74HC74E	DUAL D FLIP-FLOPS
U	11	UON0-00708	1	24355	AD708JN	AD708JN;DUAL OP AMP
U	12	UON0-00708	1	24355	AD708JN	AD708JN;DUAL OP AMP
U	14	UON0-00708	1	24355	AD708JN	AD708JN;DUAL OP AMP
U	15	UTN0-00022	1	18714	74HC02E	QUAD 2 INPUT NOR GATE
U	16	UTN0-00091	1	01295	SN74LS09N	74LS09 QUAD AND GATES
U	17	UVNP-00100	1	24355	AD587JQ	AD587;10V REF
U	18	ULN0-05053	1	32293	IH5053CJE	IH5053 QUAD ANALOG SWITC
U	19	UON0-00708	1	24355	AD708JN	AD708JN;DUAL OP AMP
U	20	UIN0-07547	1	24355	AD7547KN	AD7547KN;DUAL 12 BIT DAC
U	21	UON0-00708	1	24355	AD708JN	AD708JN;DUAL OP AMP
U	22	UON0-00708	1	24355	AD708JN	AD708JN;DUAL OP AMP
U	23	ULN0-05043	1	32293	IH5043CPE	IH5043CPA DUAL SPDT SW
U	24	UTN0-01232	1	01295	SN74HC123	RETRIG. MULTIVIBRATOR
U	25	UON0-05532	1	18324	NE5532N	DUAL;OP AMP;10MHz
U	26	UTN0-01542	1	01295	SN74HC154	DECODERS/DEMULTIPLEXER
U	27	UTN0-02732	1	01295	74HC273	74HC273;OCTAL D-TYPE F-F
U	28	UTN0-02732	1	01295	74HC273	74HC273;OCTAL D-TYPE F-F
U	29	UTN0-02442	1	04713	MC74HC244N	74HC244 8X DRIV/RECV
U	32	UIN0-07547	1	24355	AD7547KN	AD7547KN;DUAL 12 BIT DAC
U	33	UIN0-07547	1	24355	AD7547KN	AD7547KN;DUAL 12 BIT DAC
U	34	UIN0-07547	1	24355	AD7547KN	AD7547KN;DUAL 12 BIT DAC
U	35	UIN0-07547	1	24355	AD7547KN	AD7547KN;DUAL 12 BIT DAC
U	36	UON0-00708	1	24355	AD708JN	AD708JN;DUAL OP AMP
U	37	UON0-00708	1	24355	AD708JN	AD708JN;DUAL OP AMP
U	38	UON0-00708	1	24355	AD708JN	AD708JN;DUAL OP AMP
U	39	UON0-00708	1	24355	AD708JN	AD708JN;DUAL OP AMP
U	40	ULN0-00004	1	PMI	CMP04FP	CMP04;QUAD COMPARATOR
U	41	ULN0-00004	1	PMI	CMP04FP	CMP04;QUAD COMPARATOR
U	42	ULN0-00004	1	PMI	CMP04FP	CMP04;QUAD COMPARATOR
U	43	ULN0-00004	1	PMI	CMP04FP	CMP04;QUAD COMPARATOR
U	44	UTN0-01382	1	01295	SN74HC138	74HC138 DECODER/DEMULTIP
U	45	UCN0-04078	1	01295	SN74HC4078	74HC4078;8 IN NOR GATE
U	46	UIN0-07547	1	24355	AD7547KN	AD7547KN;DUAL 12 BIT DAC
U	47	UON0-00708	1	24355	AD708JN	AD708JN;DUAL OP AMP

Bill of Material (by Ref Designator)

Parts List For: 120BA06510 LEVEL PCA REV: E

Item	Part Number	Qty	Mfgr	Mfr's Part Number	Description
0	120BS06510	0.000			LEVEL SCH
1	120CP06510	1.000			LEVEL PCB
2	ETST-06224	4.000	USECO	1280B-1	TURRET TERMINAL
3	HQIP-00180	2.000	BIVAR	104-020 PERM-O-P	TO18 INSULATOR
101	HBPP-44005	3.000	NYLOK	NS137CR440R5	4-40 X 5/16 PAN
102	HWFS-40400	3.000			#4 X 1/4 FLAT WASHER
103	HWSS-40300	3.000			#4 X 3/16 SPLIT LOCK
A 10A1	120BA15520	0.000			LEVEL DRIVER PCA
C 1	CC50-03470	1.000	KEMET	C320C473K5R5CA	.047 UF CERAMIC X7R
C 2	CC50-02100	1.000	AVX	SR155C122MAT	.001 UF CERAMIC Y5P
C 3	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 4	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 5	CE25-R6470	1.000	PANSON	ECEA1EU470	47 UF 25V RADIAL LEAD
C 6	CE25-R6470	1.000	PANSON	ECEA1EU470	47 UF 25V RADIAL LEAD
C 7	CE25-R6470	1.000	PANSON	ECEA1EU470	47 UF 25V RADIAL LEAD
C 8	CE25-R6470	1.000	PANSON	ECEA1EU470	47 UF 25V RADIAL LEAD
C 9	CC50-01150	1.000	KEMET	C315C151K1G5CA	150 PF CERAMIC NPO
C 10	CC50-01150	1.000	KEMET	C315C151K1G5CA	150 PF CERAMIC NPO
C 11	CC50-01200	1.000	CENTRE	150-100-COG-201J	200 PF CERAMIC NPO
C 12	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 13	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 14	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C	CC50-02470	1.000	KEMET	C315C472K5R5CA	.0047 UF CERAMIC X7R
C	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 21	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 22	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 23	CC50-00150	1.000	KEMET	C315C150J2G5CA	15 PF CERAMIC NPO
C 24	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 25	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 26	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 27	CC50-02150	1.000	KEMET	C320C152J1G5CA	1500 PF CERAMIC
C 28	CC50-02150	1.000	KEMET	C320C152J1G5CA	1500 PF CERAMIC
C 29	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 30	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 31	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 32	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 33	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 34	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 37	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 38	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 39	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 40	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 41	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 42	CC50-00330	1.000	KEMET	C315C330J2G5CA	33 PF CERAMIC NPO
C 46	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U

Parts List For: 120BA06510 LEVEL PCA REV: E

Item	Part Number	Qty	Mfgr	Mfr's Part Number	Description
C 47	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 48	CC50-00150	1.000	KEMET	C315C150J2G5CA	15 PF CERAMIC NPO
C 49	CC50-02100	1.000	AVX	SR155C122MAT	.001 UF CERAMIC Y5P
C 52	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 53	CE16-R6330	1.000	NICHI1	UVP1C330MDAMAA	33 UF >16V NON-POL RADIA
C 54	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 55	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 56	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 57	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 59	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 60	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 61	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 62	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 63	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 64	CE25-R6470	1.000	PANSON	ECEA1EU470	47 UF 25V RADIAL LEAD
C 65	CE25-R6470	1.000	PANSON	ECEA1EU470	47 UF 25V RADIAL LEAD
C 66	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 67	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 68	CE25-R6470	1.000	PANSON	ECEA1EU470	47 UF 25V RADIAL LEAD
C 69	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 70	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 71	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 73	CC50-02100	1.000	AVX	SR155C122MAT	.001 UF CERAMIC Y5P
C 75	CC50-02470	1.000	KEMET	C315C472K5R5CA	.0047 UF CERAMIC X7R
C 76	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 77	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 78	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 79	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 85	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 86	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 87	CC50-04100	1.000	KEMET	C322C104M5U5CA	.1 UF CERAMIC Z5U
C 88	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 89	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 90	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 91	CC50-03100	1.000	TDK	RD30HX7R103K	.01 UF CERAMIC X7R
C 92	CC50-00680	1.000	KEMET	C315C680J2G5CA	68 PF CERAMIC NPO
CR 1	DSA0-04148	1.000	ANY	1N4148	1N4148 G.P. DIODE
CR 2	DSA0-04148	1.000	ANY	1N4148	1N4148 G.P. DIODE
CR 3	DSA0-02810	1.000	HP	5082-2810	5082-2810 SCHOT. DIODE
CX 74	CC50-?????	0.000			COMPONENT SELECTED IN TEST
DS 1	ILRR-10125	1.000	HP	HLMP-K101	RED LED
J 3	JIB2-20170	1.000	SAMTEC	SLW-110-01-S-D	20 PIN STRIPLINE SOCKET
J 4	JIB2-20170	1.000	SAMTEC	SLW-110-01-S-D	20 PIN STRIPLINE SOCKET
J 5	JIB2-20170	1.000	SAMTEC	SLW-110-01-S-D	20 PIN STRIPLINE SOCKET

Parts List For: 120BA06510 LEVEL PCA REV: E

Item		Part Number	Qty	Mfgr	Mfr's Part Number	Description
L	1	LAD0-06470	1.000	DALE	IMS-5 47UH 10%	47 UH INDUCTOR
L	2	LAD0-06470	1.000	DALE	IMS-5 47UH 10%	47 UH INDUCTOR
L	3	LAD0-07100	1.000	DALE	IMS5 100UH	100 UH INDUCTOR
Q	1	QMNS-00215	1.000	TOPAZ	AD215DE	SD215DE D-MOS FET
Q	2	QMNS-00215	1.000	TOPAZ	AD215DE	SD215DE D-MOS FET
R	1	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R	2	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R	3	RAPG-12000	1.000	BOURNS	3296Z-1-202	2K 10% 25T .5W POT.
R	4	RAPG-12000	1.000	BOURNS	3296Z-1-202	2K 10% 25T .5W POT.
R	5	RAPG-21000	1.000	BOURNS	3296Z-1-103	10K 10% 25T .5W TRIM POT
R	6	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R	7	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R	8	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R	10	RN50-11000	1.000	DALE	RNC50H1001F	1.00 K OHMS 1% MET FILM
R	11	RN50-11000	1.000	DALE	RNC50H1001F	1.00 K OHMS 1% MET FILM
R	12	RN50-11000	1.000	DALE	RNC50H1001F	1.00 K OHMS 1% MET FILM
R	13	RN50-11000	1.000	DALE	RNC50H1001F	1.00 K OHMS 1% MET FILM
R	14	RN50-11000	1.000	DALE	RNC50H1001F	1.00 K OHMS 1% MET FILM
R	17	RN50-11000	1.000	DALE	RNC50H1001F	1.00 K OHMS 1% MET FILM
R	18	RN50-03320	1.000	DALE	RN50C3320F	332 OHMS 1% METAL FILM
R	19	RN50-11000	1.000	DALE	RNC50H1001F	1.00 K OHMS 1% MET FILM
R	20	RN50-11000	1.000	DALE	RNC50H1001F	1.00 K OHMS 1% MET FILM
R		RN50-16980	1.000	DALE	RN50C6981F	6.98 K OHMS 1% MET FILM
R	22	RN50-16980	1.000	DALE	RN50C6981F	6.98 K OHMS 1% MET FILM
R	23	RN50-11000	1.000	DALE	RNC50H1001F	1.00 K OHMS 1% MET FILM
R	24	RN50-11000	1.000	DALE	RNC50H1001F	1.00 K OHMS 1% MET FILM
R	25	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R	26	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R	27	RAPG-15000	1.000	BOURNS	3296Z-1-502	5K 10% 25T .5W TRIM. POT
R	28	RAPG-21000	1.000	BOURNS	3296Z-1-103	10K 10% 25T .5W TRIM POT
R	29	RAPG-15000	1.000	BOURNS	3296Z-1-502	5K 10% 25T .5W TRIM. POT
R	30	RAPG-21000	1.000	BOURNS	3296Z-1-103	10K 10% 25T .5W TRIM POT
R	31	RN50-05620	1.000	DALE	RN50D5620F	562 OHMS 1% METAL FILM
R	32	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R	33	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R	34	RN50-11000	1.000	DALE	RNC50H1001F	1.00 K OHMS 1% MET FILM
R	35	RN50-11000	1.000	DALE	RNC50H1001F	1.00 K OHMS 1% MET FILM
R	36	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R	37	RN50-41000	1.000	DALE	RN50C1004F	1.00 M OHMS 1% MET FILM
R	38	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R	39	RN50-11000	1.000	DALE	RNC50H1001F	1.00 K OHMS 1% MET FILM
R	40	RN50-11210	1.000	ROHM	CRB20FX1211	1.21 K OHMS 1% MET FILM
R	41	RN50-12210	1.000	DALE	RN50C2211F	2.21 K OHMS 1% MET FILM
R	42	RN50-16980	1.000	DALE	RN50C6981F	6.98 K OHMS 1% MET FILM
R	43	RN50-22000	1.000	DALE	RN50C2002F	20.0 K OHMS 1% MET FILM

Parts List For: 120BA06510 LEVEL PCA REV: E

Item	Part Number	Qty	Mfgr	Mfr's Part Number	Description
R 44	RN50-16980	1.000	DALE	RN50C6981F	6.98 K OHMS 1% MET FILM
R 45	RN50-22000	1.000	DALE	RN50C2002F	20.0 K OHMS 1% MET FILM
R 46	RN50-11000	1.000	DALE	RNC50H1001F	1.00 K OHMS 1% MET FILM
R 47	RN50-31000	1.000	DALE	RN50C1003F	100 K OHMS 1% MET FILM
R 48	RAPG-21000	1.000	BOURNS	3296Z-1-103	10K 10% 25T .5W TRIM POT
R 49	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R 50	RAPG-25000	1.000	BOURNS	3296Z-1-503	50K 10% 25T POT
R 51	RN50-00511	1.000	DALE	RN50C51R1F	51.1 OHMS 1% METAL FILM
R 52	RN50-31000	1.000	DALE	RN50C1003F	100 K OHMS 1% MET FILM
R 53	RN55-12210	1.000	DALE	RN55C2211F	2.21 K OHMS 1% MET FILM
R 54	RN50-11000	1.000	DALE	RNC50H1001F	1.00 K OHMS 1% MET FILM
R 55	RN50-11000	1.000	DALE	RNC50H1001F	1.00 K OHMS 1% MET FILM
R 56	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R 57	RN50-13320	1.000	DALE	RN50C1332F	3.32 K OHMS 1% MET FILM
R 58	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R 59	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R 60	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R 61	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R 62	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R 63	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R 64	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
R 65	RN50-21000	1.000	DALE	RN50C1002F	10.0 K OHMS 1% MET FILM
5	RN50-32000	1.000	DALE	RN50C2003F	200 K OHMS 1% MET FILM
^ 68	WJIB-05022	1.000	3M	923345-05-C	.5 INSULATED JUMPER
R 69	RN50-12210	1.000	DALE	RN50C2211F	2.21 K OHMS 1% MET FILM
RX 9	RN50-?????	0.000			COMPONENT SELECTED IN TEST
RX 15	RN50-?????	0.000			COMPONENT SELECTED IN TEST
RX 16	RN50-?????	0.000			COMPONENT SELECTED IN TEST
U 1	UTN0-00042	1.000	ANY	74HC04	SN74HC04 HEX INVERTER
U 2	ULN0-05053	1.000	MAXIM	DG412DJ	IH5053 QUAD ANALOG SWITC
U 3	UON0-00746	1.000	ANALOG	AD746AQ	AD746JN DUAL OP AMP
U 5	UON0-00712	1.000	ANALOG	AD712JN	AD712JN DUAL OP AMP
U 6	UON0-00746	1.000	ANALOG	AD746AQ	AD746JN DUAL OP AMP
U 7	UON0-00746	1.000	ANALOG	AD746AQ	AD746JN DUAL OP AMP
U 8	ULN0-00539	1.000	ANALOG	AD539KN	AD539 LINEAR MULT/DIVIDR
U 9	ULN0-00539	1.000	ANALOG	AD539KN	AD539 LINEAR MULT/DIVIDR
U 10	UON0-00842	1.000	ANALOG	AD842JN	AD842 80 MHZ OP AMP
U 13	UON0-00746	1.000	ANALOG	AD746AQ	AD746JN DUAL OP AMP
U 14	ULN0-05053	1.000	MAXIM	DG412DJ	IH5053 QUAD ANALOG SWITC
U 15	UON0-00027	1.000	ANALOG	ADOP27GN	OP27GN LOW DRIFT OP AMP
U 16	ULN0-05053	1.000	MAXIM	DG412DJ	IH5053 QUAD ANALOG SWITC
U 17	UON0-00712	1.000	ANALOG	AD712JN	AD712JN DUAL OP AMP
U 18	ULN0-05053	1.000	MAXIM	DG412DJ	IH5053 QUAD ANALOG SWITC
U 19	ULN0-00311	1.000	TI	LM311P	LM311N COMPARATOR
U 20	UTN0-01382	1.000	TI	74HC138N	74HC138 DECODER/DEMULTIP

Bill of Material (by Ref Designator)

Parts List For: 120BA06510 LEVEL PCA REV: E

Item	Part Number	Qty	Mfgr	Mfr's Part Number	Description
U 21	UTN0-02732	1.000	TI	74HC273N	74HC273;OCTAL D-TYPE F-F
U 22	UTN0-02732	1.000	TI	74HC273N	74HC273;OCTAL D-TYPE F-F
U 23	UTN0-01252	1.000	TI	SN74HC125AN	MC74HC125N QUAD BUFFER
U 24	UIN0-07846	1.000	ANALO	AD7846JN	AD7846JN;16 BIT DAC
U 25	UON0-00708	1.000	ANALO1	AD708JN	AD708JN DUAL OP AMP
U 26	UVNP-00050	1.000	PMI	PMI REF02HP	REF02 5V 3PPM REFERENCE
U 27	UON0-00027	1.000	ANALOG	ADOP27GN	OP27GN LOW DRIFT OP AMP
U 28	ULN0-00539	1.000	ANALOG	AD539KN	AD539 LINEAR MULT/DIVIDR
U 29	UON0-00746	1.000	ANALOG	AD746AQ	AD746JN DUAL OP AMP
U 30	UON0-00027	1.000	ANALOG	ADOP27GN	OP27GN LOW DRIFT OP AMP
U 31	UIN0-07524	1.000	MAXIM	MX7524JN	AD7524 8 BIT D/A
U 32	UON0-00072	1.000	TI	TL072CP	TL072CP DUAL FET OP AMP
VR 1	DRAE-00827	1.000	MOT	1N827A	1N827 6.2V REF. DIODE
VR 2	DRAE-00827	1.000	MOT	1N827A	1N827 6.2V REF. DIODE
VR 3	DZAD-04728	1.000	MOTO	1N4728	IN4728 3.3 V ZENER
Y 1	Y180-00246	1.000	NEL	NEL C1360N	2.4576MHZ CRYSTAL